Faculty of Engineering and Technology

Master Program in Electrical Engineering

Modeling and Control of Shunt Active Power Filter in Medium Voltage applications

By:

Wafa I. S. Qutaina

Supervisor:

Dr. Muhammad Abu-Khaizaran

Master Thesis Submitted to Birzeit University in Partial Fulfillment the Requirement of Master Degree in Electrical Engineering

May-2019

Abstract:

This thesis introduces design, modeling, control strategies and improving safety performance of Shunt Active Power Filter (SAPF) in Medium Voltage (MV) applications for power quality (PQ) improvement issues. Random harmonics and transients generated by grid-tied inverters and non-linear loads, such as different types of power electronic converters, will be reduced, also the reactive power, voltage levels and power factor will be adjusted using the SAPF. This thesis is focused on implementing different topologies of SAPF such as; two level and multilevel SAPF inverters (basically Neutral Point Clamped-NPC inverters). The research will focus on the performance and effects of using different control techniques , in particular, proportional-integral (PI controllers) and Hysteresis Current Controllers (HCC). The aim of the study is to provide a comparison between these different topologies and control techniques. Besides. The study will demonstrate the ability of various schemes in compensating the Total Harmonic Distortion (THD), correcting the power factor up to unity, decreasing the losses in SAPF inverter by choosing a suitable element values (DC-Link voltage level, DC capacitance and coupling inductor values), which leads to decreasing the physical size of the passive components in SAPF. In addition, the study will focus on the SAPF performance under different operational cases, such as make a discrimination between the starting current (inrush current) and the fault current by determining the second harmonic ratio method ,which leads to improving the safety performance of SAPF, real case study is also performed after collecting real data of MV grid. *MATLAB/SIMULINK* software package will be used in conducting the study, comparing and displaying the results**.**

الملخص:

الغاية من أطروحة الماجستير هو دراسة تصميم, أساليب التحكم و زيادة الأمان في أداء مرشحات القدرة الفعالة (SAPF) في تطبيقات الشبكات ذات الجهد المتوسط بغرض معالجة قضايا معايير وجودة القدرة (Power Quality). القضايا التي ستتم معالجتها هي التوافقيات العشوائية و الموجات العابرة التي تنتج من عاكسات الطاقة المربوطة على الشبكة، الاحمال غير الخطية كمحولات الكترونيات القوى. كما سيتم استخدام مرشحات القدرة الفعالة كمصدر للقدرة غير الفعالة التي تستخدم لتعديل مستوى الجهد في الشبكات الكهربائية و ذلك عبر ضبط معامل القدرة على مختلف القيم. هذه الرسالة تركز على استعمال مختلف أنواع العاكسات المستخدمة في مرشحات القدرة الفعالة كالعاكسات ذات المستويين والعاكسات متعددة المستويات (بشكل أساسي نوع NPC) مع دراسة أثر أداء مختلف أساليب التحكم والسيطرة مثل المتحكم التناسبي-التكاملي (PI) و المتحكم المقارن (HCC). هدف هذه الدراسة هو عمل مقارنة بين مختلف أنواع الدوائر و أساليب التحكم المستخدمة في مرشحات القدرة الفعالة من حيث مستوى قابليتها في تقليل مستوى التشوه الكلي (THD) و ترشيحه, تحسين معامل القدرة و رفعه حتى قيمة الوحدة الواحدة, تقليل الخسائر في مرشحات القدرة عبر اختيار القيم المناسبة للعناصر المكونة للمرشح (الاختيار الانسب لمستوى الجهد على بسبار الجهد المستمر الموجود في مدخل المرشح، اختيار قيمة مواسعة المكثف المستخدم في بسبار الجهد المستمر و اختيار القيمة المناسبة لمحاثة الملف المستخدم على خرج المرشح) الامر الذي سيساهم في تقليل الحجم الفيزيائي للمرشح المقترح، كما ستتم دراسة أداء المرشح المقترح في مختلف بيئات التشغيل لزيادة موثوقية المرشح و امان تشغيله كدراسة حماية المرشح في حالة الحمل الزائد، دراسة مسألة التمييز بين تيارات البدء (Inrush Current) و تيارات القصر (Fault Current) عبر تحديد نسبة التوافقية الثانية، كما سيتم اختبار أداء المرشح لدراسة مسالة ترشيح التوافقيات لحالة حقيقية و ذلك بعد جمع بياناتها على الجهد المتوسط. سيتم استخدام برنامج المحاكاة *(MATLAB/SIMULINK)* لاجراء الدراسة والمقارنات المطلوبة بغرض عرض النتائج وتحليلها.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

LIST OF ABBREVIATIONS

APF	Active Power Filter
CSI	Current Source Inverter
CB	Circuit Breaker
DBHCC	Double Band Hysteresis Current Controller
FC	Flying Capacitor
FFT	Fast Fourier Transform
HB	Hysteresis Band
HCC	Hysteresis Current Controller
IGBT	Insulated-Gate Bipolar Transistor
LCL	Inductance-Capacitance-Inductance Filter
MV	Medium Voltage
NPC	Neutral Point Clamp
P_{ac}	Power of harmonics (dissipated by other than the fundamental frequencies)
P_{avg}	Average Power (dissipated by fundamental frequency)
PCC	Point of Common Coupling
PPF	Passive Power Filter
PF	Power Factor
PI	Proportional-Integral
PID	Proportional-Integral-Derivative
PL	Real Power of Load
PPF	Passive Power Filter
PQ	Power Quality
P-Q	Instantaneous Reactive Power Theory
PV	Photovoltaic
PWM	Pule Width Modulation
QL	Reactive Power of Load
SAPF	Shunt Active Power Filter
SBHCC	Single Band Hysteresis Current Controller

SMPS	Switch Mode Power Supply
THD	Total Harmonic Distortion
VSI	Voltage Source Inverter
VSAPF	Voltage Source Active Power Filter
CSAPF	Current Source Active Power Filter
CCVSI	Current Controlled Voltage Source Inverter

Chapter One

Introduction

1.1 Introduction:

In an ideal power system, power should be transferred from the source to the customer as pure sine waves for voltages and currents. But in practice, that does not happen due to the existence of non-linear loads such as power electronic converters that add a wide range of harmonic distortion into utility grid.

Power electronic converters act as non-linear loads due to the switching operation that occur within them. Inserting these converters lead to generating random harmonics into the utility grid, which causes a poor power quality. Furthermore, using power electronic converters with high inductive loads lead to decrease the power factor level [1], [2]. These poor power quality problems add unnecessary losses to utilities, and can cause electrical hazards in electrical equipment, such as transformers, underground cables and meters.

To mitigate power quality problems, which are mainly high Total Harmonic Distortion (THD) and poor power factor, two main solutions are proposed: (i) passive filters and (ii) active power filters. These filters are still in optimization process and the new trends focus on implementing multilevel inverters in Active Power Filters with different control techniques.

1.2 Objectives:

The objectives of this thesis are to:

1. Study and develop high effective and reliable grid conditioning circuits to solve poor power quality issues such as; harmonic compensation, power factor correction and transients.
2. Comparing the performance of different control techniques such as PI and Hysteresis Current Controllers.

3. Comparing the performance of different circuit topologies, mainly two level and multilevel inverters.
4. Develop SAPF to Adapt the grid's PF.
5. Study the Adaptive DC-link voltage effect in different conditions.
6. Develop a protection system against overload, fault and irush cases.
7. Make a discrimination between Fault and inrush current.

1.3 Report Layout :

This thesis is organized in seven chapters. Chapter Two reviews related literature and previous work about SAPF. In Chapter Three, modeling and methodologies of SAPF are presented. Chapter Four describes how to design SAPF parameters. Chapter Five describe new purposes of SAPF. Chapter Six presents SAPF simulation and discuss its performance and results. Finally, Conclusions and Future work are addressed in Chapter Seven.

Chapter Two

APF Literature Review

2.1 Introduction

Installation of various types of power electronic converters and nonlinear loads such as AC/DC rectifiers, variable frequency drives and soft starters, is the major cause of PQ problems (high THD%, poor power factor and different types of transients). Therefore, it is crucial to evaluate new solutions in order to increase the quality of the electrical services by reducing the harmonics distortion, correcting the power factor and reducing the losses.

Recently, a tremendous research focused on delivering real power to the loads, in addition to mitigating harmonics and increasing the power factor up to unity, which may cause problems associated with resonance and stability. APFs become the most effective solution in eliminating different types of harmonics (inter-harmonics and sub-harmonics) due to their advantages such as; fast response to grid variations, ability to compensate random harmonics and high control accuracy [8].

In practice, APF injects a compensating current or voltage into the Point of Common Coupling (PCC) equal but opposite in its direction to the grid's harmonics in order to cancel a wide range of harmonics that affect the system, also it generates / absorbs reactive power into PCC in order to correct grid's power factor (PF). Furthermore, APF keeps the grid system balance and stable with load variations and grid transients. Fig. 2.1 shows the general operating concept of APF [9].

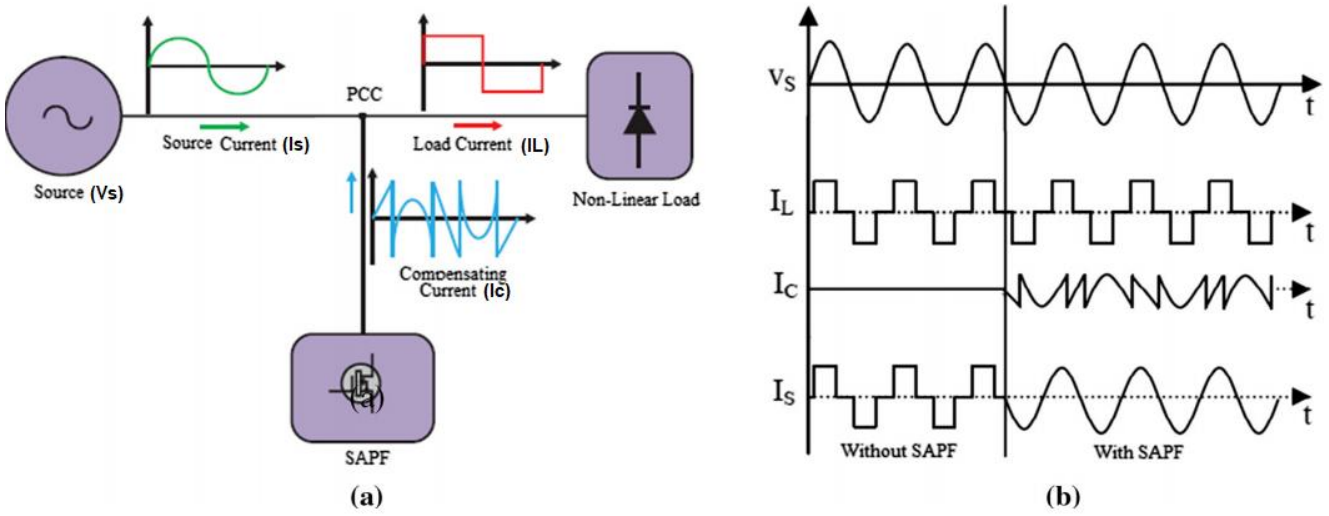

Fig. 2.1: General working concept of Active Power Filters; (a) block diagram of SAPF and (b) respective waveforms [9].

2.2 ***Power Quality Issues and Standards***

Power quality (PQ) is defined according to IEEE dictionary as "the concept of powering and grounding sensitive equipment in a matter that is suitable to the operation of that equipment" [2]. Power quality is a set of parameters that is related to the harmonic distortion levels, voltage levels, power factor and wave shape quality.

Harmonic content is a very important parameter in power grids that is caused by non-linear loads such as electronic rectifiers, switch mode power supplies (SMPS), electronic ballast, AC derives and soft starters. This harmonic content causes high additional losses in grids equipment such as; transmission lines and transformers, which may lead to make hazards in these components [10], [11]. To organize PQ issues, IEEE-519 is the most famous standard that shows the allowable Total Harmonic Distortion (THD) limits for voltage and Total Demand Distortion (TDD) for current in medium voltage applications (there is no standard for THDi in MV applications). Table I shows the voltage harmonic distortion levels according to IEEE-519 [12]. Table II shows the current harmonic distortion levels according to IEEE-519 [12].

Table I: Voltage harmonic distortion levels according to IEEE-519.

Bus Voltage at PCC	**Individual harmonics (%)**	**Total Harmonic Distortion THD (%)**
V ≤ 1 KV	5.0	8.0
1 KV < V ≤ 69 KV	3.0	5.0
69 KV < V≤ 161 KV	1.5	2.5
161 KV < V	1.0	1.5
NOTE: High-voltage systems can have up to 2.0% THD where the cause is an HVDC terminal that will attenuate by the time it is tapped for a user.		

Table II: Current harmonic distortion levels according to IEEE-519.

Maximum Harmonic Current Distortion in Percent of IL						
Individual Harmonic Order (Odd Harmonics)						
I_{SC}/I_L	3≤h<11	11≤h<17	17≤h<23	23≤h<35	35≤h<50	TDD_I
<20*	4.0	2.0	1.5	0.6	0.3	5.0
20<50	7.0	3.5	2.5	1.0	0.5	8.0
50<100	10.0	4.5	4.0	1.5	0.7	12.0
100<1000	12.0	5.5	5.0	2.0	1.0	15.0
>1000	15.0	7.0	6.0	2.5	1.4	20.0
Even harmonics are limited to 25% of the odd harmonic limits above.						
Current distortions that result in a DC offset, e.g. half-wave converters, are not allowed.						
* All power generation equipment is limited to these values of current distortion, regardless of actual Isc/IL.						
Where Isc = maximum short-circuit current at PCC. IL = maximum demand load current (fundamental frequency component) at PCC. PCC = Point of Common Coupling.						

IEEE-519 defines the limit of Total Harmonic Distortion of voltage (THDv) in MV applications to be 5%, and suggests calculating tables for current's Total Demand Distortion (TDDi) depending on the ratio of short circuit capacity to the rated current in utility grids (usually it is 5% in distribution companies).

2.3 ***Passive Vs Active Filters****.*

There are three types of filters; passive, active and hybrid filters. Each type has its own classifications as follows:

A- Passive Filter:

It is a low pass filter that consists of passive elements (resistors, inductors or capacitors). This type of filter is simple in design and cheap in low power applications. The main drawbacks of this types are tuning difficulties, its inability to compensate the sub-harmonics (harmonics with a frequency below 50 Hz), resonance problems, in addition to its low efficiency, high cost and bulky size in high power applications [13]. Fig. 2.2 shows the main circuit topologies of passive filters [14].

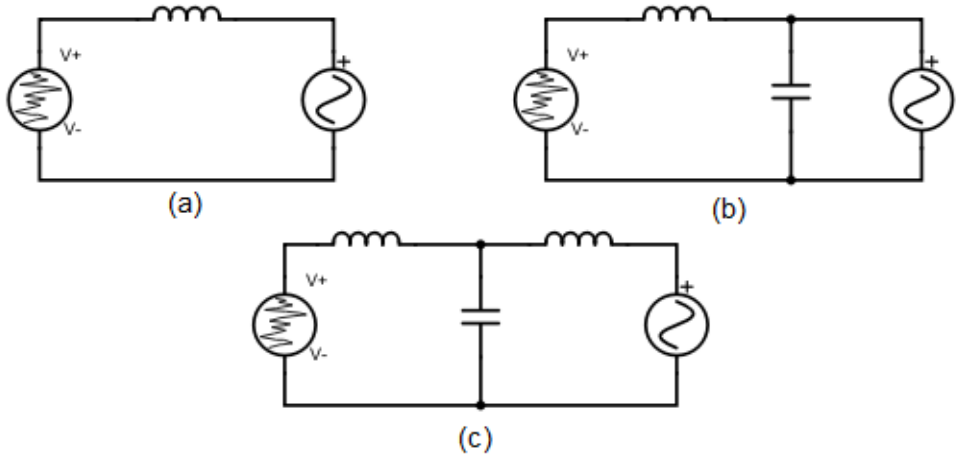

Fig. 2.2: Main circuit topologies of passive filters; (a) L, (b) LC and (c) LCL types [14].

B- Active Filter:

It is an electronic filter that consists of active elements (transistor switches, diodes) with complex control techniques. This type of filters has a high efficiency, more complex in its design, providing an isolation property, accurate in Power Factor (PF) correction, acting as a load balancer, which is used in high power applications and accurate systems, such as airplanes, and it is able to compensate the all types of harmonics [13].

C- Hybrid Filters

It is a combination between passive and active filters, the main advantage of this type is significantly reducing the rating of active filters in addition to achieving a harmonic isolation between supply and loads in utility grids [13]. Fig. 2.3 shows the main configuration of hybrid filters [13].

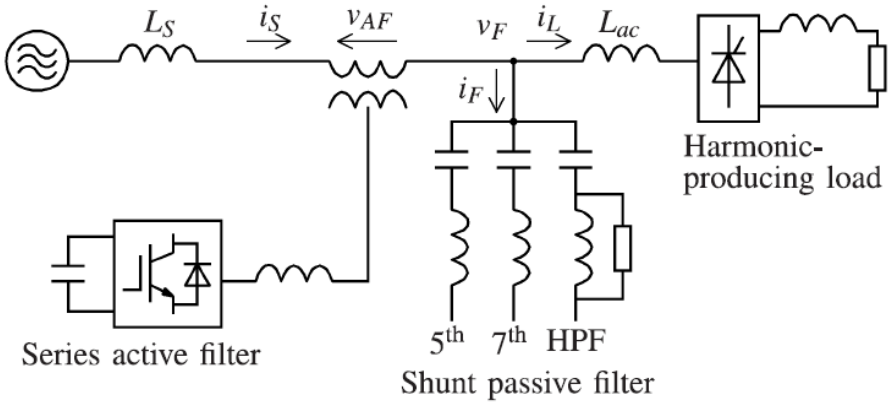

Fig. 2.3: The main configuration of hybrid filters.

2.4 ***Active Power Filters***

There are two main types of Active Power Filters (APF); Series Active Power Filters and Shunt Active Power Filters. Each type has its own properties and applications.

A- Series Active Power Filter

It is a filter used in series with the load and it is designed to mitigate voltage harmonics of the grid by generating negative voltage harmonic in order to cancel the effects of the load voltage harmonics, It keeps the grid's voltage in a pure sine shape against transients such as sag and ,swell and flicker events in addition to balancing the unbalanced voltage source [6], [15]. Fig. 2.4 shows the topology of a Series APF.

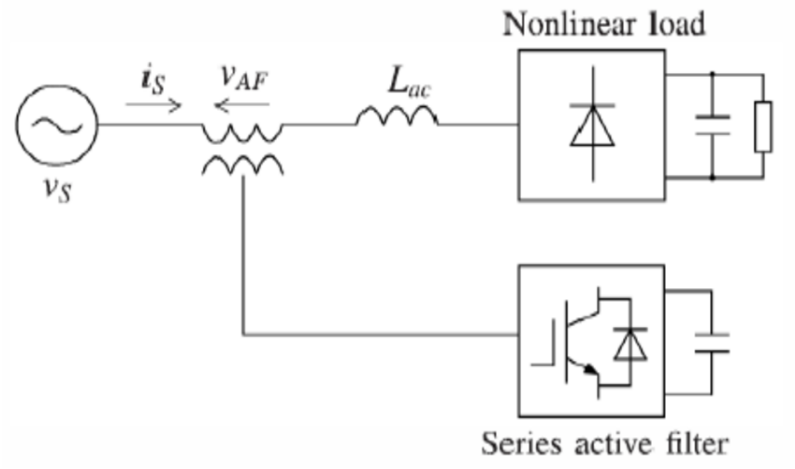

Fig. 2.4: A series Active Power Filter Configuration.

B- Shunt Active Power Filter

It is a filter connected in parallel with nonlinear loads that used to reduce the grid's current distortion, and to increase the utility power factor by injecting negative harmonic currents into the grid in order to achieve a pure sine wave in addition to balancing the unbalanced loads [15]. Fig. 2.5 shows the topology of a Shunt Active Power Filter (SAPF).

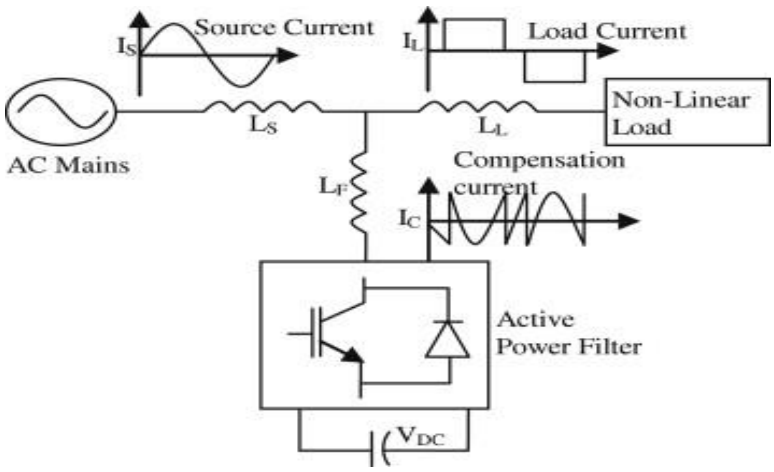

Fig. 2.5: Shunt Active power filters configuration.

The main drawback of the Series APF is that, it has to handle the high load current (handle with the same current rating of the load), which leads to increasing the current rating of this type [15], It might cause protection coordination problems that appear by adding costly linking transformer in series with utility. This will cause miscoordination problems and increasing the tripping time of Circuit Breakers (CB). Since MV grids usually suffer from current distortion more than voltage distortion. Shunt type is commonly used as an Active Power Filter since it works as current compensator with lower effects on protection coordination system and lower in costs, as it is transformerless.

The literature shows that, using Voltage Source Active Power Filter (VSAPF) is more efficient than using Current Source Active Power Filter (CSAPF) in low and medium power applications in terms of power loss and THDi reduction, while CSAPF is better in high power applications [16]. CSAPF needs additional overvoltage protection in DC-link inductor in the case of transients. Both types have significant losses, the main losses in VSAPF is in it's AC-linking inductance filter while the losses in CSAPF is in its DC-link inductance. Fig. 2.6 shows the basic topology of VSAPF and CSAPF [16].

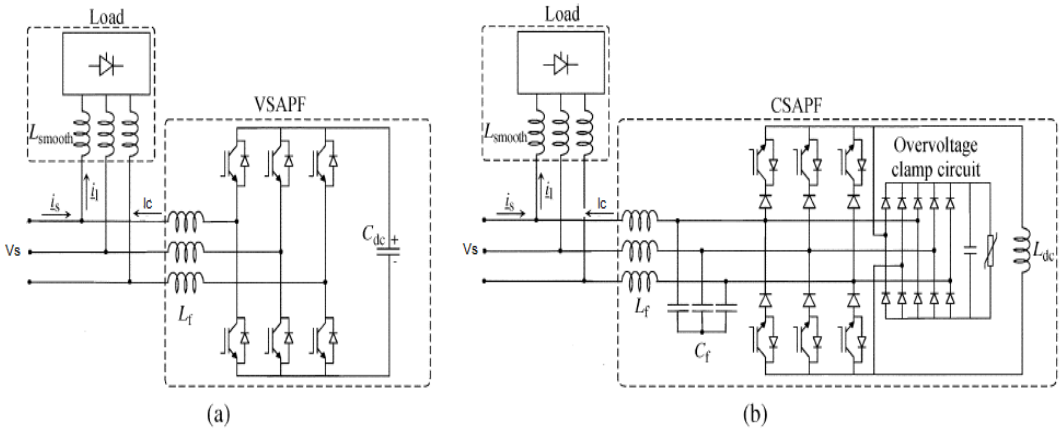

Fig. 2.6: Basic topology of : (a) VSAPF, (b) CSAPF.

2.5 ***New Trends in APF***

Recent research in the field of SAPF focuses on increasing efficiency, improving performance and reliability in different grid conditions and transients. The new research trends are classified into four main categories:

A. Double Band Hysteresis Current Controllers (DBHCC):

The Hysteresis Current Controller could be single or double band. The Single Band Hysteresis Current Controller (SBHCC) is a current limiter controller used to keep an error signal within a specific band. The main disadvantage of this type is its high switching losses that may damage the switching devices [17], [18]. Fig. 2.7 illustrates the operating principle of SBHCC [18]. On the other hand, the Double Band Hysteresis Current Controller (DBHCC) is a method that is used to overcome the drawbacks of SBHCC in terms of reducing switching losses and THD [17], [18]. Fig. 2.8 illustrates the operating principle of DBHCC [18]. Adaptive Hysteresis Current Controllers (AHCC) are also used to overcome the drawbacks of SBHCC by inserting adaptive system of hysteresis band in order to keep the switching frequency constant [18].

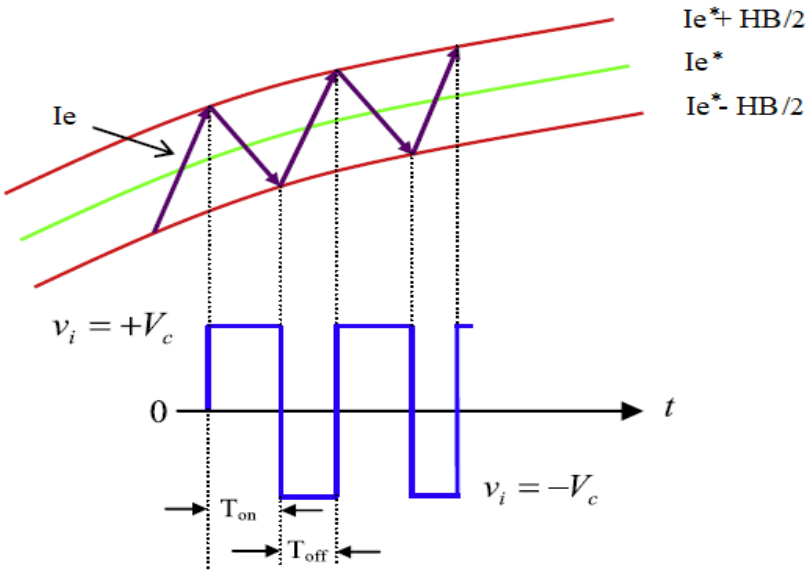

Fig. 2.7: Operating principle of Single Band Hysteresis Current Controller (SBHCC).

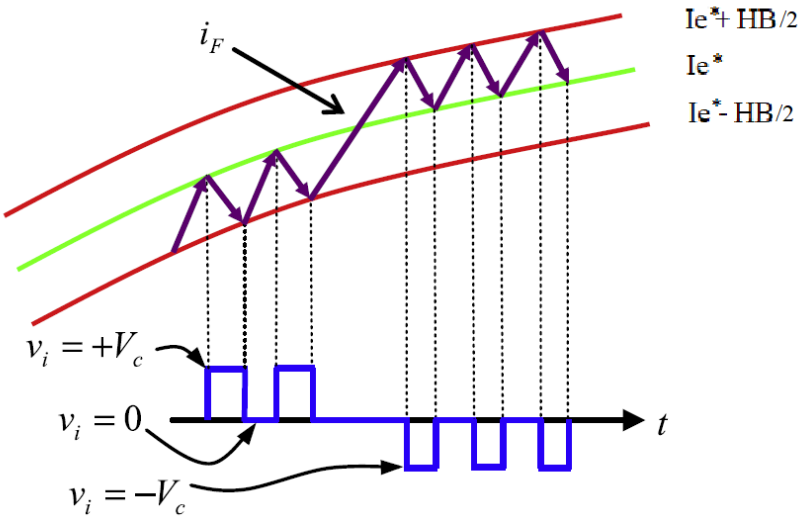

Fig. 2.8: Operating principle of Double Band Hysteresis Current Controller (DBHCC).

B. SAPF with LCL filters:

Implementation of SAPF with LCL filter at the output of inverter's bridge has many advantages, such as decreasing the inductance value, in comparison with the classical L filter, which leads to decreasing SAPF size, in addition to making the SAPF more stable [19]. However, using an LCL filter at the output of inverter may cause lagging in phase and resonant transients in case of unity PF operation; when the inductive reactance of the load equals the capacitance reactance of LCL filter, $X_{L\_Load} = X_{C\_LCL}$, which is considered as a disadvantage [20]. There are many damping circuits which can be used to avoid the drawbacks of using an LCL filter at the output of the SAPF. These damping circuits are difficult to design and calibrate, because the SAPF generates currents in a wide harmonic spectrum range [20]. Fig. 2.9 shows different damping circuits of LCL filters inserted at the out of SAPF.

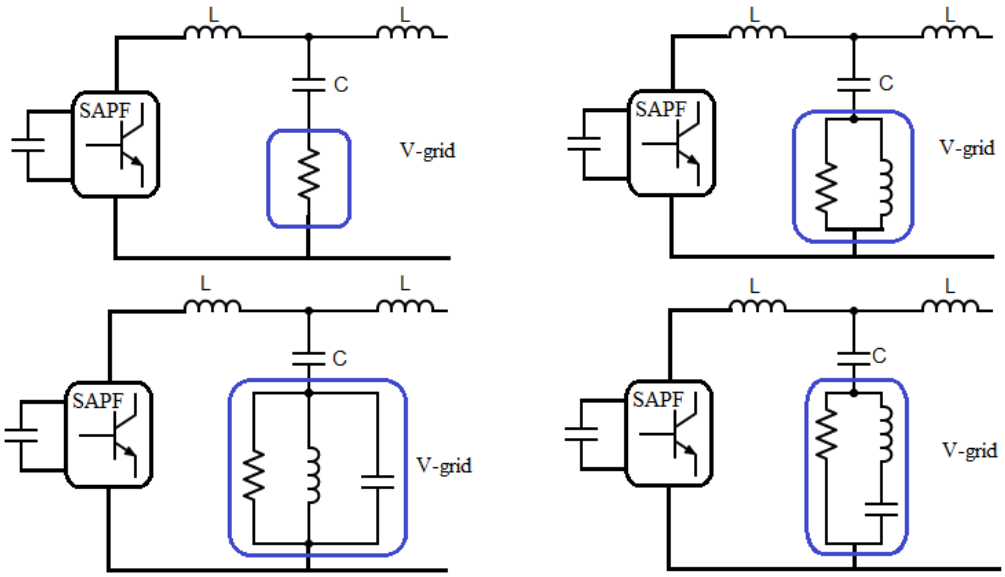

Fig. 2.9: Different damping circuits used with LCL filters.

C. Parallel Operation of SAPF:

This method relies on inserting two parallel SAPF into the utility grid with 180º phase shift between two carrier frequencies from each other. These two inverters share the same DC-Link capacitor in order to reduce the voltage stress on the DC bus. The main benefit of this method is decreasing the

THD down to 62% of single SAPF THD value, and decreasing the DC-link capacitor value significantly up 70% of single SAPF capacitor value [21]. Fig. 2.10 shows the parallel APF block diagram.

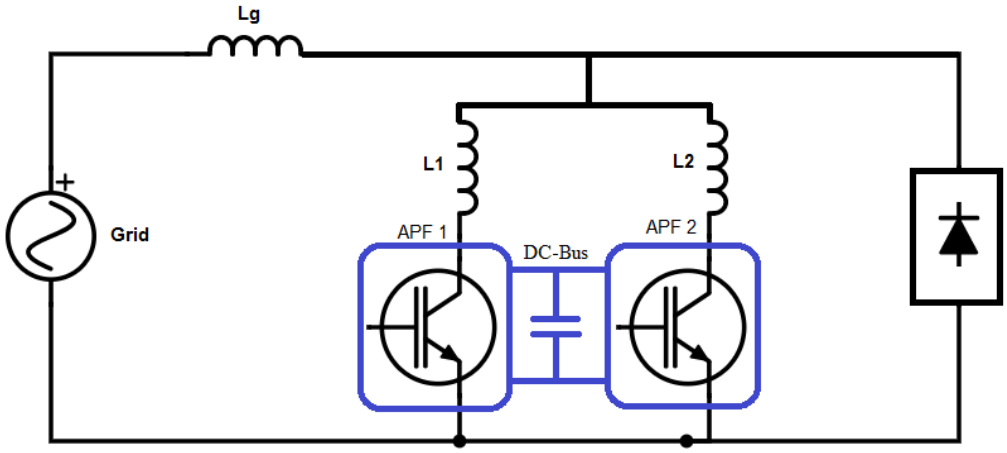

Fig. 2.10: Parallel SAPF block diagram

D. New Current controller techniques such as Genetic Algorithms (GA), Artificial Neural Network (ANN), Particle Swarm Optimization (PSO), wavelet theory, sliding mode and negative sequence current controllers, which are reviewed in detail [22].

Chapter Three

Modeling and Methodology

3.1 Methodologies of SAPF

SAPF is a three-phase voltage source inverter that is used to stabilize the system's performance, by generating specific reference current for the IGBT Bridge (or any other switches) in order to mitigate random harmonics and compensate the PF up to unity. SAPF can reduce the grid's losses in transformers and cables by correcting the PF and cancelling harmonics, in addition to decrease the voltage drop in long transmission lines, instead of using costly booster transformers [23]. SAPF will increase the capacity of substations to deliver the rated power as a real power, so the SAPF can decrease the outage periods in cases of limited available capacity (taking Palestine as an example) [23].

There are several methods to evaluate reference signals in frequency and time domain. The main methods which are discussed in a review paper, [24], are classified as follows:

A- Frequency domain; Fast Fourier Transform Method (FFT)

B- Time domain:

(i) Sinusoidal subtraction

(ii) Synchronous reference frame (dq theory)

(iii) Instantaneous reactive power theory (P-Q theory)

Literature review shows that the main drawback of FFT method is its bad performance in transients. FFT samples must be taken within one cycle and any transient in the current waveform will cause an error in the output compensating current. To avoid that, SAPF must be shut down during transient conditions [24]. Sinusoidal subtraction method also has the same drawback as that of the FFT [24]. The main drawback of d-q theory is its need for Phase Locked Loop (PLL), which needs a careful implementation in the case of unbalanced voltage source [25]. P-Q theory is the best choice for SAPF implementation since it does not need a PLL and it has a good performance during transient conditions [25].

3.2 Instantaneous Reactive Power (P-Q) Theory

In a P-Q theory, the reference current calculation depends on measuring the three phase voltages and currents, then converting them into two-phase model (α-β) by Clarke transformation method. These two-phase reference currents are used to generate the gate signals of the inverter bridge after evaluating the three phase reference currents by inverse Clarke transformation, which is discussed in [8]. Fig. 3.1 illustrates a block diagram of reference signals calculation depending on P-Q theory. Fig. 3.2 shows the overall transfer matrices that show the detailed calculation procedure, which will be discussed later.

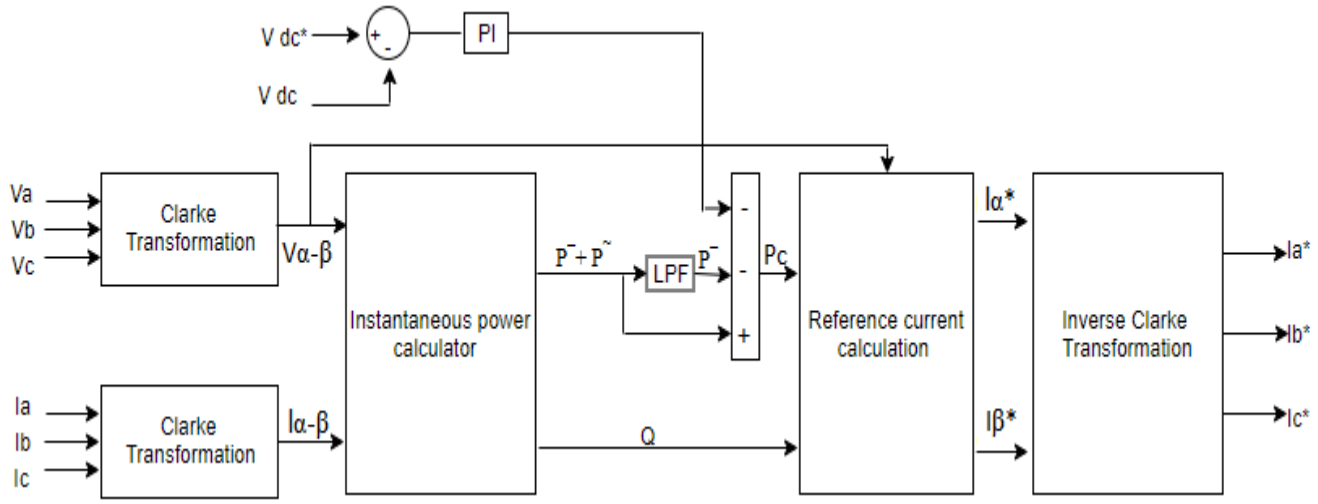

Fig. 3.1: Block diagram of P-Q theory for a reference current calculation.

where $P^{\sim}$ and $Q^{\sim}$ are real and reactive power consumed by frequencies other than the fundamental frequency, respectively.

DC voltage regulator here is used to adapt DC-link voltage on pre-determined or adapted value, the error in DC-link voltage is directly proportional to the losses in DC-link due to DC voltage variations that may occur in DC-link, which must be considered in harmonics power calculation.

In steady state: $Pc = P^{\sim} = P - P^{-}$

In DC-link voltage variation: $Pc = P^{\sim} = P - P^{-} - P_{loss}$

The DC-link PI controller can be adapted either by calculating the transfer function or by trial and error, second method used to find PI parameters in this thesis.

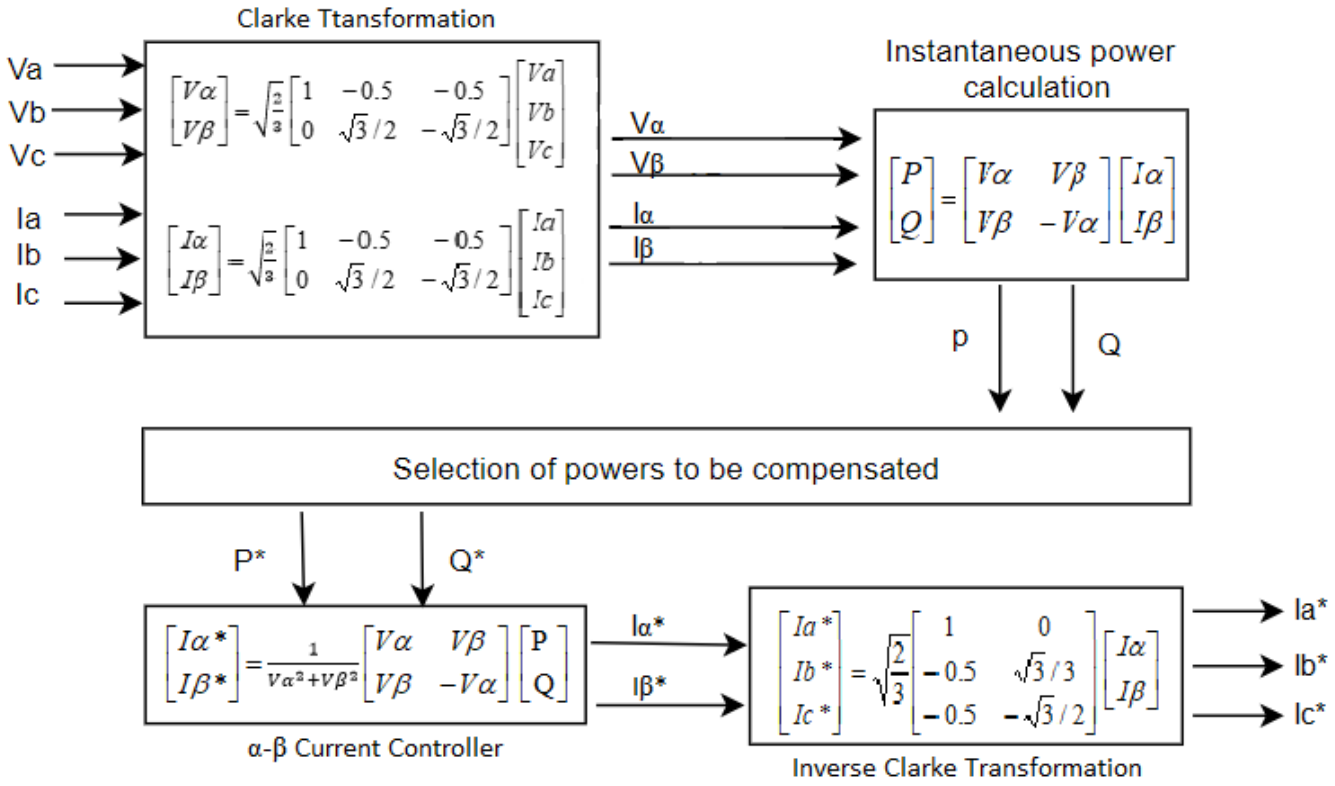

Fig. 3.2: Overall transfer matrices for reference signals generation.

3.3 ***Modeling of P-Q Theory***

Several steps are taken to model P-Q theory:

A. Two Phase Calculation:

Two-phase calculation method is used to convert the three-phase measurements into a two-phase model (α & β) using Clarke transform according to Eq. (3.1). This way simplifies the calculations, and enables separation between real and reactive power controllers [26].

$$\begin{bmatrix} V\alpha \\ V\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -0.5 & -0.5 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} Va \\ Vb \\ Vc \end{bmatrix} \quad \ldots(3.1)$$

$$\begin{bmatrix} I\alpha \\ I\beta \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -0.5 & -0.5 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} Ia \\ Ib \\ Ic \end{bmatrix}$$

B. Instantaneous Power Calculation:

Both of instantaneous real power (P) and instantaneous reactive power (Q) include two components; an average power component due to the fundamental component of the load current (50 Hz) and an AC power component corresponding to harmonic currents of the load (at frequencies other than 50 Hz). This instantaneous powers can be calculated by implementing Eq. (3.2) [26].

$$\begin{bmatrix} P \\ Q \end{bmatrix} = \begin{bmatrix} V\alpha & V\beta \\ V\beta & -V\alpha \end{bmatrix} \begin{bmatrix} I\alpha \\ I\beta \end{bmatrix} \quad \ldots(3.2)$$

where:

$P = \bar{P} + \tilde{P}$

$Q = \bar{Q} + \tilde{Q}$

Such that $\bar{P}$ and $\bar{Q}$ are the average components of real and reactive powers, respectively, that are consumed at the fundamental frequency (50 Hz). Whilst $\tilde{P}$ and $\tilde{Q}$ are the AC components of real and reactive powers, respectively, that are consumed at frequencies other than 50 Hz.

C. Selection of The Power to be Compensated:

After calculating real and reactive powers of the utility grid, as mentioned previously in Eq. (3.2), the reference AC real power ($\tilde{P}$) can be calculated by extracting the fundamental average power ($\bar{P}$) from total power (P). The fundamental power can be evaluated by applying a low pass filter on the total power signal as was illustrated in Fig. 3.1. This method divides the total power (P) into two separate

components ($\bar{P}$ & $\tilde{P}$), and select the AC component only to be compensated. For a unity PF, all the reactive power (Q) has to be compensated without dividing it into sub-components.

D. Reference Current Calculation in Two Phase Model:

The reference compensating currents I_a* and I_b* in a two-phase model can be calculated depending on Eq. (3.3) [26].

$$\begin{bmatrix} I\alpha* \\ I\beta* \end{bmatrix} = \frac{1}{V\alpha^2+V\beta^2} \begin{bmatrix} V\alpha & V\beta \\ V\beta & -V\alpha \end{bmatrix} \begin{bmatrix} \mathrm{P} \\ \mathrm{Q} \end{bmatrix} \quad \ldots(3.3)$$

These reference currents in the two-phase system represent the desired compensating currents for the inverter bridge.

E. Three-Phase Reference Current Calculation:

The compensating current in a three-phase model is mandatory for a three-phase inverter, and can be evaluated from Eq. 3.3 by applying inverse Clarke transformation according to Eq. (3.4) [26].

$$\begin{bmatrix} Ia* \\ Ib* \\ Ic* \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & 0 \\ -0.5 & \sqrt{3}/3 \\ -0.5 & -\sqrt{3}/2 \end{bmatrix} \begin{bmatrix} I\alpha* \\ I\beta* \end{bmatrix} \quad \ldots(3.4)$$

3.4 ***Current Controller Techniques:***

These control techniques are used to force the compensated current out of SAPF inverter (Ia, Ib and Ic) to follow the calculated reference current (Ia*, Ib* and Ic*) with a small error value, and there are two main control strategies:

1- Hysteresis Current Control Technique:

It is one of the common current control methods, where the actual current is forced to follow its reference current. Technically, this method limits the actual current between two boundaries equally displaced from the reference. It does not let the actual current to leave the band between the boundaries by turning the inverter's switches ON or OFF. The main drawback of this method is its

high switching frequency, which leads to high switching losses and may cause hazards for the inverter. This type of controllers is applicable in low power inverters [17]. Fig. 3.3 shows the operating principle of Hysteresis Controllers.

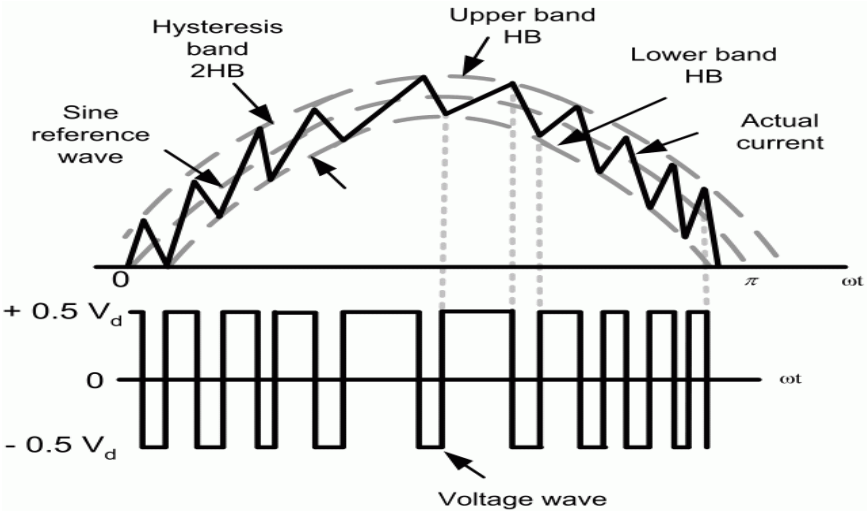

Fig. 3.3: Operating principle of Hysteresis Controller [17].

When the error value exceeds the upper band, the upper switch turns ON and the lower switch turns ON, and when the error signal exceeds the lower band, the upper switch turns ON and the lower switch turns OFF [27].

$$S = \begin{cases} 0, & error > upper\ HB \\ 1, & error < lower\ HB \end{cases}$$

2- PID Control Technique:

A proportional–Integral–Derivative (PID) controller is a kind of generic feedback control. The widespread use of PID-controllers can recently be seen in the industry. A PID-controller computes an "error" as the difference between a desired value and an actual value. It helps in optimizing the systems performance and minimizing the error by adjusting the controller gains. The main advantage of this type of controllers is its low switching losses [27]. Fig. 3.4 shows a PID block diagram. Eq. (3.5) describes the main function of the PID controller. The components of a PID controller are:

- Proportional (P): It is responsible for error amplitude, which can be adjusted by multiplying it with a gain factor.
- Integral (I): It is used to eliminate the steady state error signal and decreasing the regulation time (rising time), by integrating the error signal.
- Derivative (D): It is used to improve the dynamic response by deriving the error and producing a signal proportional to the rate of change of the error signal.

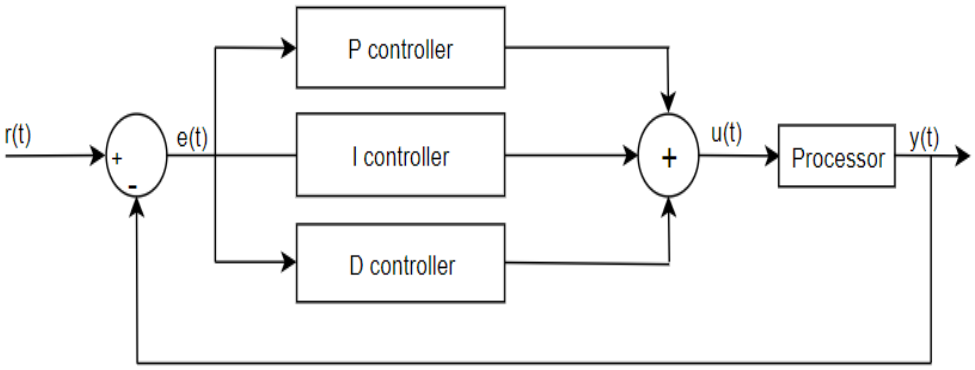

Fig. 3.4: A Block diagram of PID controller.

$$Y(t) = Kp * e(t) + Ki * \int_0^t e(t) + Kd * \frac{d\,e(t)}{dt} \quad \ldots(3.5)$$

3.5 Power Processor Types:

A SAPF is a three-phase Inverter that can be a Voltage Source Inverter (VSI), a Current Source Inverter (CSI), and a Current Controlled Voltage Source Inverter (CCVSI). There are many topologies of inverters, which can be classified as follows [28]:

A. Two Level Inverter: It uses 6 IGBT in a Bridge. This type of inverters is used in low-voltage and low-power applications such as; small factories, robotics and aerospace applications. Fig. 3.5 shows a two-level inverter topology.

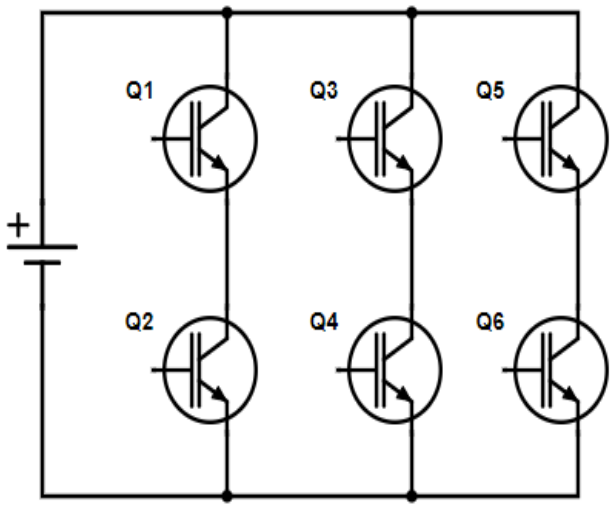

Fig. 3.5: A two-level inverter topology.

B. Multilevel Inverter: It is a multistep inverter that provides several voltage levels. This type of inverters is used in medium-voltage and high-power applications such as; utility grids, substation filters, motor drives and in large factory applications. There are three main types of multilevel inverters, each topology has its advantages and disadvantages.

-Diode Clamped Multilevel Inverter (called Neutral Point Clamped (NPC)): NPC inverter was firstly introduced by Nabai, Takashi and Akagi in 1981 [28]. Fig. 3.6 shows a three level Diode Clamped inverter (one leg). The main advantages of this type is its simplicity in construction and sharing the same DC-Link voltage bus. On the other hand, the main problems of the Converter is the voltage balancing problem across the series capacitors at high modulation levels. In addition, the voltage blocking across each clamping diode varies depending on its position in the inverter, which is another problem [28].

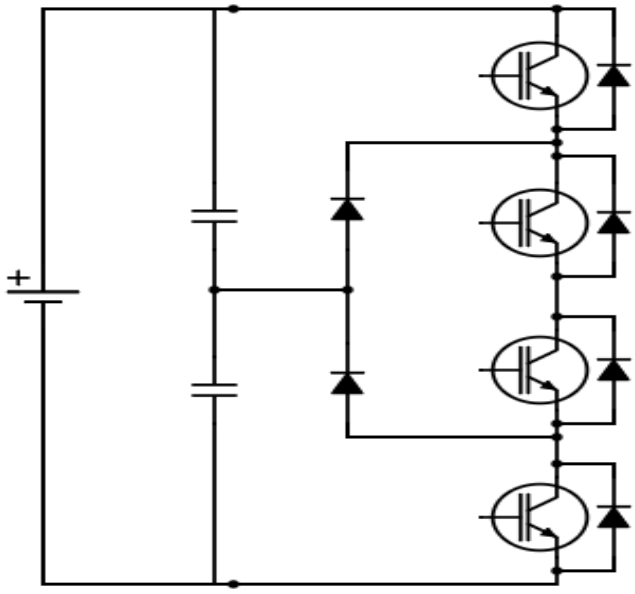

Fig. 3.6: A single leg of a three-level Diode Clamped inverter.

- Flying Capacitor Multilevel Inverter (FC): FC inverter was firstly introduced by Meynard in 1992 [28]. This type of inverters overcome the drawbacks of NPC type, and proposes a solution for voltage balancing problem [28]. Fig. 3.7 shows the three level flying capacitor inverter (one leg). The main drawbacks of this inverter are high voltage and high current ripple in each capacitor, capacitor inrush current, bulky and high cost [28], [29].

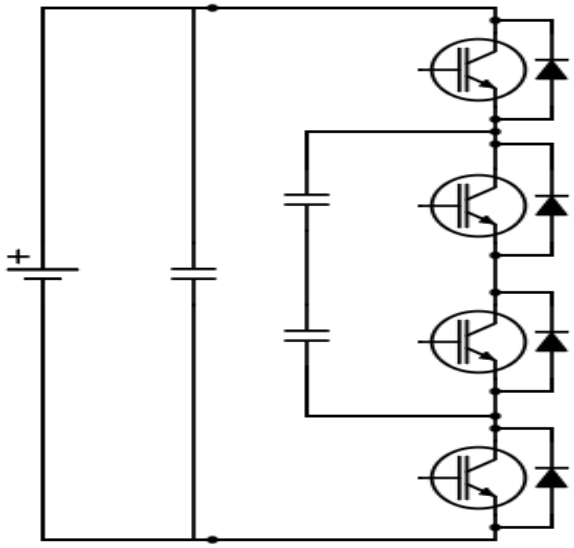

Fig. 3.7: A single leg of a Three-level Flying Capacitor Inverter.

- Cascaded H-Bridge Multilevel Inverter: This topology is based on a series connection of H-Bridges (modular form). Fig. 3.8 shows a five-nine level Cascaded Inverter bridge. Cascaded H-Bridge inverter has a simple structure with its separate DC source, has the ability to operate under partial failure, due to its modularity, and it is suitable for renewable energy projects [27].

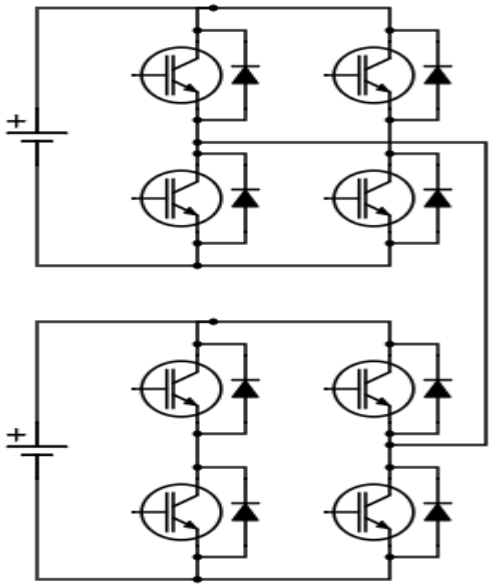

Fig. 3.8: A single phase of a five-nine level Cascaded Inverter.

Neutral Point Clamp (NPC) is commonly used in power application, since it has a simple structure and contains only one common DC-bus, it needs only one voltage stabilizer at the DC-bus side. The main drawback of a Cascaded H-Bridge Multilevel inverter is its needed for separate voltage sources, therefore more than one voltage stabilizer is needed. Flaying Capacitor (FC) type has a high current ripple in each clamping capacitor, which is considered as a disadvantage of this type.

These inverters has three main signal generating strategies:

- Level Shift Control Technique: using level shifting (DC shifting) of carrier signals.
- Phase Shift Control Technique: using time shifting of carrier signals.
- Space Vector Control Technique: it is a method used for PWM generation, mainly used in AC Drives applications.

Level shift and phase shift methods provides a pre-determined switching frequency (specific carrier frequency). Level shift method commonly used in multilevel inverters, while phase shift method is suitable for parallel operation applications (parallel inverters with phase shift in carrier frequency). Anyway, level shift method will be used in this thesis.

Chapter Four

SAPF PARAMETERS Design

The quality of SAPF performance depends on an accurate design of filter components. In recent years, there are several designing methods of SAPF parameters such as; DC-link voltage (V_{DC}), coupling inductance (L_C) and DC-link capacitor (C_{DC}). All of the design parameters are calculated based on the following assumptions [30]:

- A sinusoidal voltage source
- PWM inverters are operating in the linear region (0<M<1; where M is the modulation index)

4.1 DC-Link Voltage Design (V_{DC})

4.1.1 First Method:

According to [30] and [31], V_{DC} must be greater than the peak voltage of the grid's voltage in order to get a good controllability of the inverter to compensate random harmonics.

$$V_{\mathrm{DC}} > \frac{\sqrt{2}*\sqrt{3}*Vs}{\mathrm{M}} \qquad \ldots(4.1)$$

where;

Vs: the Phase voltage of the source

M: the maximum value of the modulation index in the PWM scheme.

4.1.2 Second Method:

This method firstly introduced by Mohan in 1989 [32] and discusses later in [33] and [34]. This method is based on the fact that the practical value of coupling inductance (L_f) is small in high frequency applications (SAPF is high switching frequency converter). This makes the voltage out of inverter approximately equal to the grid's voltage (neglecting the voltage drop cross L_f). Thus, for maximum modulation index (M=1), the reference DC-link voltage (V_{DC}) can be written as [35], [36]:

$$V_{DC} > 2 * \sqrt{2} * V_s \quad \ldots(4.2)$$

where;

Vs: the phase voltage of the source.

4.1.3 Third Method; Adaptive DC bus Voltage Reference

This Method was proposed by Musa in 2017 [30]. This method fundamentally regulates VDC depending on the output variables of SAPF by converting three phase values into d-q frame. The model of SAPF is given by:

$$L_f * \frac{di_{fd}}{dt} = L_f * \omega * i_{fq} - V_{fd} + V_{sd} = U_d \quad \ldots(4.3)$$

$$L_f * \frac{di_{fq}}{dt} = -L_f * \omega * i_{fd} - V_{fq} + V_{sq} = U_q \quad \ldots(4.4)$$

where:

Ifd: Direct component of inverter's current

Ifq: Quadrature component of inverter's current

Vfd: Direct component of inverter's voltage

Vfq: Quadrature component of inverter's voltage

Lf: Coupling inductor

Vsd: Direct component of grid's voltage

Vsq: Quadrature component of grid's voltage

ω: Angular frequency of current components (d and q)

The filter estimated voltage is given by:

$$V_{fd} = L_f * \omega * i_{fq} + V_{sd} - U_d \quad \ldots(4.5)$$

$$V_{fq} = -L_f * \omega * i_{fd} + V_{sq} - U_q \quad \ldots(4.6)$$

$$V_{f_{max}} = K * \sqrt{V_{fd^2} + V_{fq^2}} \quad \ldots(4.7)$$

$$V_{DC_{ref}} > 1.7 * \sqrt{V_{fd^2} + V_{fq^2}} \quad \ldots(4.8)$$

Fig. 4.1 shows how to implement a set of equations (Eq. 4.3 – Eq. 4.8) in order to calculate reference DC voltage.

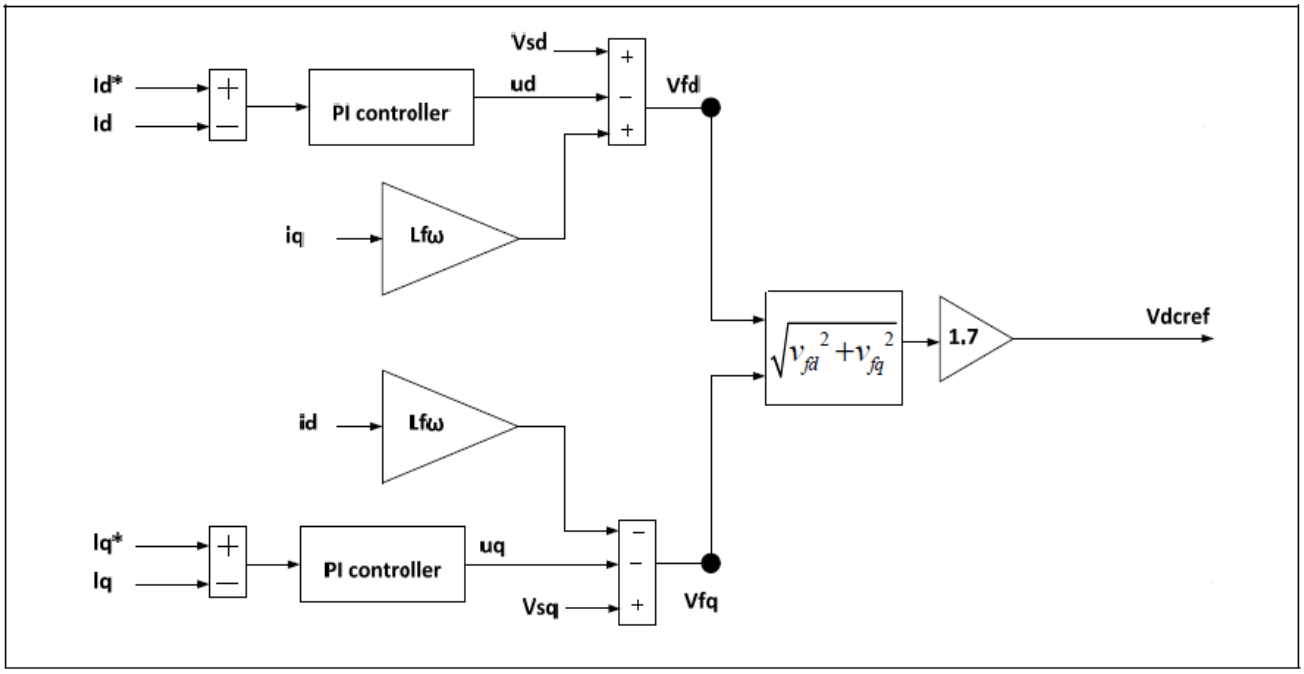

Fig 4.1: A block diagram of the DC-Bus reference voltage generation [30]

This method is better than previous estimation methods since it regulate the V_{DC} depending on load and grid variation such as; increasing load, sag and swell events. The main drawback of this method is its bad behavior during fault conditions as will be discussed later in the simulation chapter.

4.2 Coupling Inductor Design

Coupling inductor (Lf) is a very important element in SAPF. It is essential to choose its value carefully, low values of Lf add a distortion into grid's parameters, and high values of Lf impedes the compensating current from regulating the current wave shape in order to get a pure sine wave.

4.2.1 First Method:

According to [30],[37], and after assuming that the inverter's voltage and grid's voltage are equal, the coupling inductance value can be calculated by Eq. 4.9.

$$L_f = \frac{Vs}{2*\sqrt{6}*fs*\Delta Ip\_p\ max} \quad \ldots(4.9)$$

Where:

$\Delta Ip_p max$: represents 15% of SAPF peak current.

fs: switching frequency.

4.2.2 Second Method:

This method was proposed by Etxeberria in 2003 [38]. The author proposes a minimum value of coupling inductor in order to limit the maximum current ripple injected from SAPF into grid utility. The maximum current ripple can generally be calculated by:

$$\Delta I_f = \frac{\Delta V}{L_f} * \Delta t \quad \ldots(4.10)$$

Positive (T+) and Negative (T-) voltage periods of the inverter's output can be given by Eq. 4.11 and Eq. 4.12.

$$T+ = \frac{Ts}{2} * \frac{2Vs+V_{DC}}{2V_{DC}} \quad \ldots(4.11)$$

$$T- = \frac{Ts}{2} * \frac{-2Vs+V_{DC}}{2V_{DC}} \quad \ldots(4.12)$$

By substituting Eq. 4.11 and Eq. 4.12 in Eq. 4.10, yield:

$$\Delta If+ = \frac{\Delta t}{L_f} * \Delta V = \frac{T+}{L_f} * \Delta V = \frac{T+}{L_f} * \left(\frac{V_{DC}}{2} - Vs\right) = \frac{Ts}{8*Lf*V_{DC}} * (VDC^2 - 4Vs^2) \quad \ldots(4.13)$$

$$\Delta I_{f-} = \frac{\Delta t}{L_f} * \Delta V = \frac{T-}{L_f} * \Delta V = \frac{T-}{L_f} * \left(\frac{V_{DC}}{2} + Vs\right) = \frac{Ts}{8*Lf*V_{DC}} * (VDC^2 - 4Vs^2) \quad \ldots(4.14)$$

$$\Delta I_{f\_max} = \frac{Ts*VDC}{8*L_f} \quad \ldots(4.15)$$

$$L_{f\_min} = \frac{Ts*VDC}{8*\Delta I_{f\_max}} \quad \ldots(4.16)$$

4.3 ***DC-Bus capacitor Design***

This method was proposed by Chatterjee in 1999 [39]. The calculation of bus capacitor is based on the maximum power delivered to the load during worst condition (transient cases) and can be given by:

$$C = \frac{2*P\_max}{VDC^2*(1-(\frac{VDC\_min}{VDC})\text{^}2)} \quad \ldots(4.17)$$

Furthermore, there are three methods for DC-link capacitance calculation during transients and steady state conditions, which are presented in [40] and the highest value of these values must be selected.

-First Value, Step increase of fundamental current (Load increase):

$$C1 = \frac{Vm*\Delta Ic1*T}{VDC^2-VDC\_min^2} \quad \ldots(4.18)$$

where ΔIc1, is the allowable Step Current in the Utility Grid by adding new loads.

-Second Value, step decrease in the fundamental current (Load decrease):

$$C2 = \frac{Vm*\Delta Ic2*T}{VDC\_max^2-VDC^2} \quad \ldots(4.19)$$

where ΔIc2, is the allowable Step Current in Utility Grid when removing some loads.

-Third Value, steady state condition:

$$C3 = \frac{Vm*\Delta Ic2*T/2}{|\Delta VDC^2-VDC^2|} \quad \ldots(4.20)$$

where ΔIc3 is the peak current of SAPF (peak current of reactive power and harmonic compensation).

Chapter Five

SAPF Applications

SAPF's have a lot of benefits, some of the well known benefits: (i) Harmonic compensator, (ii) P.F correction and (iii) Balance the unbalanced loads. Whilst the other new benefits, which will be studied in this thesis are: (i) Adaptive P.F correction, (ii) True P.F correction, (iii) Adaptive DC-Link voltage and another important issue of the SAPF is the (iv) Safe operation during transient conditions such as: (a) Overload, (b) Fault condition, and (c) inrush conditions and how to discriminate between these transients in order to avoid disconnecting healthy feeders.

5.1 Adaptive Power Factor

Achieving a unity power factor is one of the main purposes of SAPF, but that is not needed all the time. Some applications needs a power factor to be adaptive [41], such as power factor compensation of nearby loads as shown in Fig. 5.1.

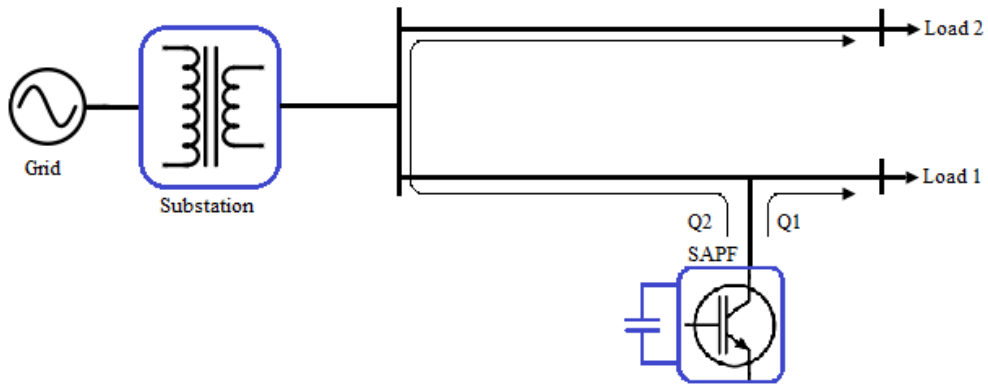

Fig. 5.1: SAPF provides reactive power to nearby load (Leading Case).

5.2 True Power Factor Correction

Power Factor (PF) or Displacement Power Factor (PF_D) are known as the ratio between the fundamental real power (P_1) to the fundamental apparent power (S_1) [42]:

$$PF_D = \frac{P_1}{S_1} \quad \ldots(5.1)$$

Harmonics existing in utility grids establish another factor called True Power Factor (PF_T), which consists of two components [42-44]:

- Displacement Power Factor (PF_D), due to the fundamental component.
- Distortion Factor (DF), which represents the effect of harmonics on power factor.

$$PF_T = PF_D * DF \quad \ldots(5.2)$$

$$DF = \frac{1}{\sqrt{1+THD^2}} \quad \ldots(5.3)$$

SAPF compensates utility harmonics (DF=1), that means it converts PF_T to a well known PF_D.

5.3 *Safe Operation of SAPF*

Safe operation of SAPF is a very important issue in order to improve it's stability. Safe operation is directly related to the protection system and discrimination between faults and transients by clearing the faults and taking the correct decision for transients.

5.3.1 Overload Protection

Overload case occurs when the compensating current exceeds the current rating of the inverter's switches and designed filter. Digital protection is used to avoiding inverter's damage that may occur. This digital protection can simply be designed by applying a digital current limiter (Digital Current Clipper) at the output of a reference current generator as shown in Fig. 5.2 [45].

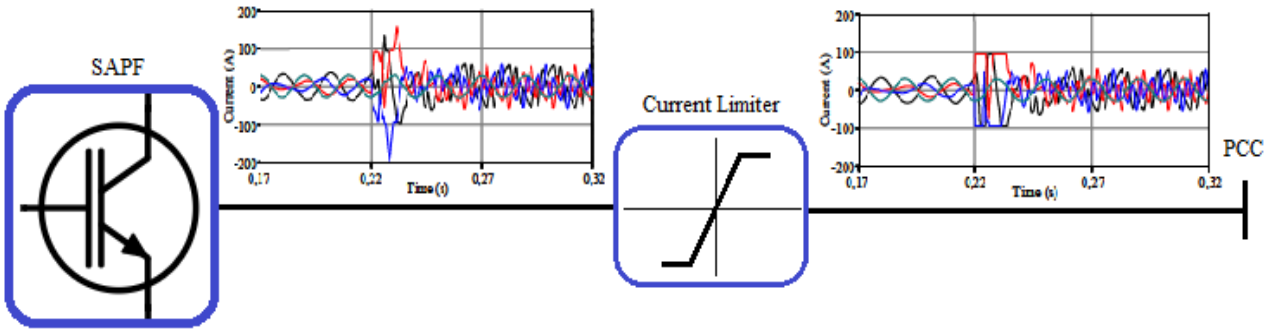

Fig. 5.2: A digital current limiter for overload protection of SAPF.

5.3.2 Short Circuit Protection

A short circuit case in a MV application may be caused by insulation failures, flashover or incorrect configuration of grid topology. Short circuit appears as overcurrent in utility grids. The value of this overcurrent depends on fault type in addition to system impedances [46]. Fault duration is divided into three sub-periods, as illustrated in Fig. 5.3 [47]:

A. Subtransient period
B. Transient Period
C. Steady-state period

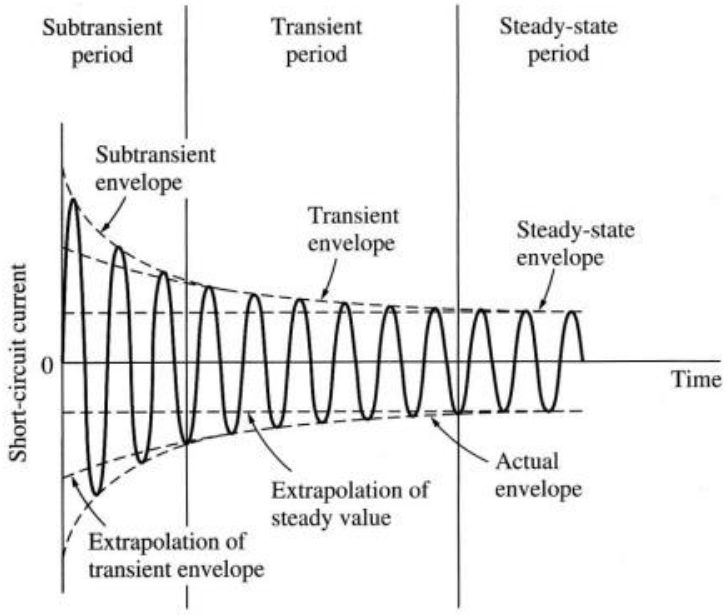

Fig. 5.3: Fault current periods.

Electrical equipment should have a short circuit capacity greater than expected Sub-transient fault level in order to avoid damaging it, protection devices need to clear faults based on predetermined time delay (for coordination purposes).

5.3.3 Inrush Current Protection

Inrush Current is an overcurrent phenomenon, which occurs at transformer energizing instant, and may cause false tripping of protection devices, such as overcurrent and differential protection relays. IEEE guide for protecting power transformers describes inrush current as "an overcurrent flow through primary winding of transformers while there is no current flow (or small value of current) in secondary winding even if there is connected load" [48]. Fig. 5.4 shows general waveform of an Inrush current.

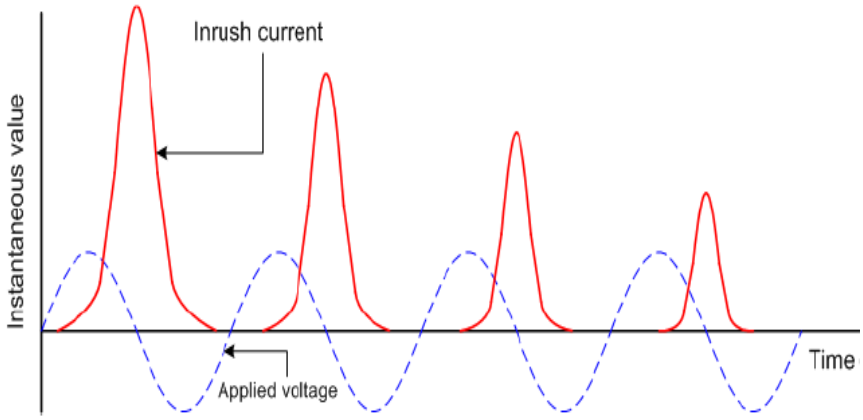

Fig. 5.4: Inrush current waveform.

Both of Fault and Inrush currents appear as overcurrent cases (inrush current can reach 10-15 times the transformer rated current for a hundreds of millisecond). Discrimination between Fault overcurrent and Inrush current can be determined by the absence of second harmonic ratio of 12-20% in inrush case (second harmonic ratio to fundamental value) [49-51]. Schneider electric Sepam protection relays adjust its second harmonic ratio of 17-20% [52].

5.4 Microprocessor Vs Mechanical Protection

There are a lot of protection equipment used in inverter applications, each one has its advantages and disadvantages such as;

-Fuse: Low cost, need to be replaced after melting, low response time in comparison with digital protection and has a low losses.

-Circuit Breakers (CB): is an automatically operated electrical switch designed to protect an electrical circuit from damage caused by excess current from an overload or short circuit, this type of protection has a very high cost in MV applications.

-Using inverter's filter (large LC filter) for transient suppressing: High costs, high losses and bulky in size.

- Microprocessor protection (Digital): has no additional costs, fast response, has no losses and transients since it make the interruption in low current circuits (reference current signals) for both of DC_Link inside inverter and AC link at PCC (soft stopping).

Chapter Six

Simulation and Results

6.1 SAPF Block Diagram and Design

In this thesis, the SAPF is operated as an active filter connected in parallel with utility grid in order to compensate random harmonics caused by nonlinear loads, many load cases are discussed in this thesis, some of these cases are theoretical, while the other cases are practical as a part of HEPCo utility. Fig. 6.1 shows the main block diagram of SAPF connected directly into MV grid (11 KV, 50 Hz).

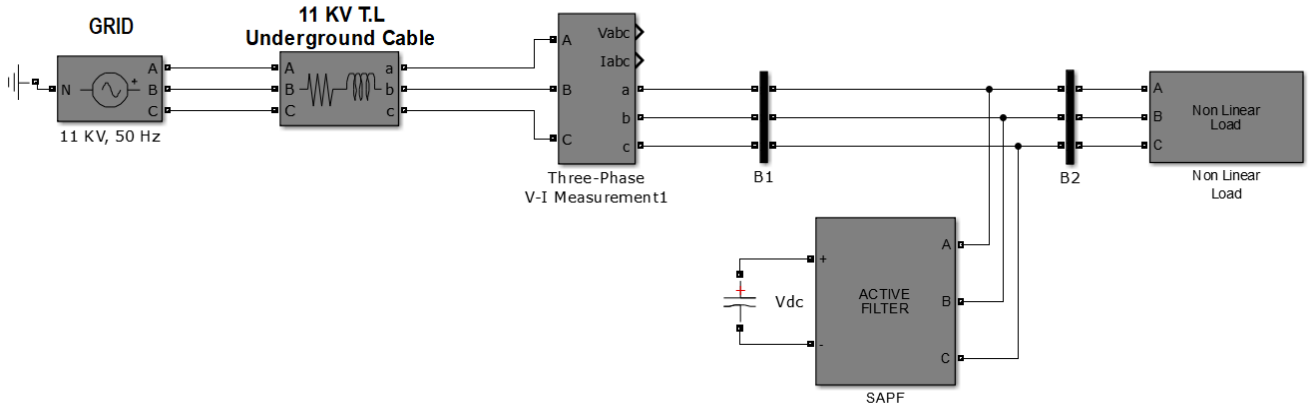

Fig. 6.1: The block diagram of a SAPF connected into a MV grid (11 KV).

where:

- The line impedance represents a transmission line of 150mm cable with length of 1 Km and has a trefoil formation (R=0.124 Ω/Km, L=0.35 mH/Km, X_L= 0.11 Ω/Km, R/X= 1.127) [53].
- The grid is a medium voltage infinite bus (substation).

Three phase AC/DC uncontrolled rectifier with RL load and smoothing capacitor (R= 68Ω, L=20mH, C=10uF, and P=3.25 MW) represents a nonlinear load that draw a wide spectrum of harmonics. Additional variable load can be used as unbalanced load. Fig. 6.2 shows the nonlinear and with adjustable Power Factor topology.

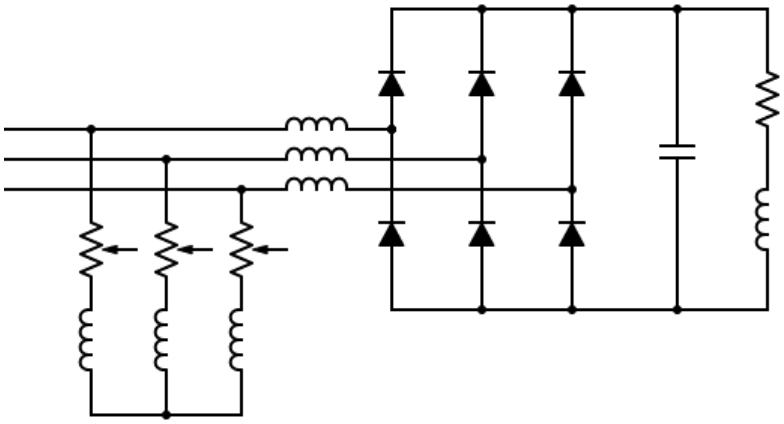

Fig. 6.2: Three phase AC/DC rectifier topology with adjustable Power Factor topology

In order to study the response of SAPF with high level of harmonic contents, there are many other types of loads that can be added in parallel to make the system full of harmonics and unbalanced such as single-phase loads, controlled AC/DC rectifiers and practically modeled loads.

In general, Table III shows the SAPF design parameters for an accurate and a reliable performance.

Table III: SAPF designed parameters

Parameter	Value	Note
VL-L	11KV	Line-to-Line Voltage
Vph	6.4KV	Phase Voltage
f	50Hz	Frequency
Simulation time	1.5s	Overall simulation time
SAPF becomes active after	100ms	SAPF become active after first five cycles

fs	20kHz	Switching Frequency of SAPF
Load Type		-Three-Phase uncontrolled AC/DC Rectifier - Practical case of HEPCO MV grid
Vo	14.855 kV	DC Voltage Out of Rectifier $V_{out} = \frac{3*\sqrt{2}}{\pi} * Vrms = \frac{3*\sqrt{2}}{\pi} * 11000 = 14.855\ kV$
RL	68Ω	Load Resistance
XL	20mH	Load Reactance
PL	3.25MW	Load Power, $P_L = \frac{(Vout)^2}{R} = \frac{(14855)^2}{68} = 3.25\ MW$
ΔI_{f_max}	15A	Allowable Current Ripple out of SAPF
VDC	25kV	$VDC > 2 * \sqrt{2} * Vs$, Vs=6.4kV , $VDC > 18.18kV$ Chose VDC greater than 18.18kV for under voltage transient purposes. Choose VDC=25KV
Coupling inductor (L)	15mH	$Lf_{min} = \frac{Ts*VDC}{8*\Delta If\_max} = \frac{(1/20000)*25000}{8*15} = 10mH$ Chose it 15mH
VDC_min	24kV	Minimum Voltage on DC bus during transient conditions
VDC_max	26kV	Maximum Voltage on DC bus during transient conditions
ΔVDC	0.5kV	Voltage Ripple on DC Bus in steady state conditions
$\Delta Ic1 = \Delta Ic2$	100A	Allowable Step Current in Utility Grid as will discuss later in this chapter (When adding new loads or removing it)
$\Delta Ic3$	400A	Peak current supplied by SAPF for reactive power and harmonic compensation (Peak current rating). (Current rating of SAPF, 400A peak)
C_1	635uF	$C_1 = \frac{Vm*\Delta Ic1*T}{VDC^2-VDC\_min^2} = \frac{11KV*\sqrt{2}*100*(\frac{1}{50})}{25KV^2-24KV^2} = 635uF$
C_2	635uF	$C_2 = \frac{Vm*\Delta Ic2*T}{VDC\_max^2-VDC^2} = \frac{11KV*\sqrt{2}*100*(\frac{1}{50})}{26KV^2-25KV^2} = 635uF$

C_3	100uF	$C_3 = \frac{Vm*\Delta Ic3*T/2}{\lvert\Delta VDC^2 - VDC^2\rvert} = \frac{11KV*\sqrt{2}*400*(\frac{1}{100})}{\lvert 0.5KV^2 - 25KV^2\rvert}$ =100uF
C	635uF	Choose C=635uF, the largest value of C1,C2 and C3.
Power Rating of SAPF		Max Current Rating= $\Delta Ic1 + \Delta Ic3$= 100+400=500A RMS rating current=$\frac{500}{\sqrt{2}} = 354A$ Rating voltage= 11KV Rating Power= $\sqrt{3}$ * I*V= $\sqrt{3}$*354*11000= 6.7MVW

6.2 Overall SAPF Simulation Block

The overall SAPF block diagram that represents a set of equations described previously in eqs. (3.1-3.4) is shown in Fig. 6.3. This block diagram consists of an instantaneous power calculator, a DC link stabilizer, a low pass filter, a compensating current controller, a pulse generator, an inverter and an inductance filter. The DC-link stabilizer is used in order to achieve a constant voltage across DC-link capacitor at the input of the inverter. The input DC voltage may obtained from a photovoltaic energy source via maximum power point tracker unit, or simple AC/DC controlled rectifier. The low pass filter is used in order to separate the compensated harmonic out of the total harmonic distortion as will be discussed later. The compensating current calculator evaluates the desired reference currents. Pulse generator block diagram consists of different current control techniques (hysteresis, PI, etc). Different types of inverters (two level or multilevel) are used in order to convert the DC voltage into AC. Finally, the inductance filter is needed as a coupling device to connect SAPF into the utility grid.

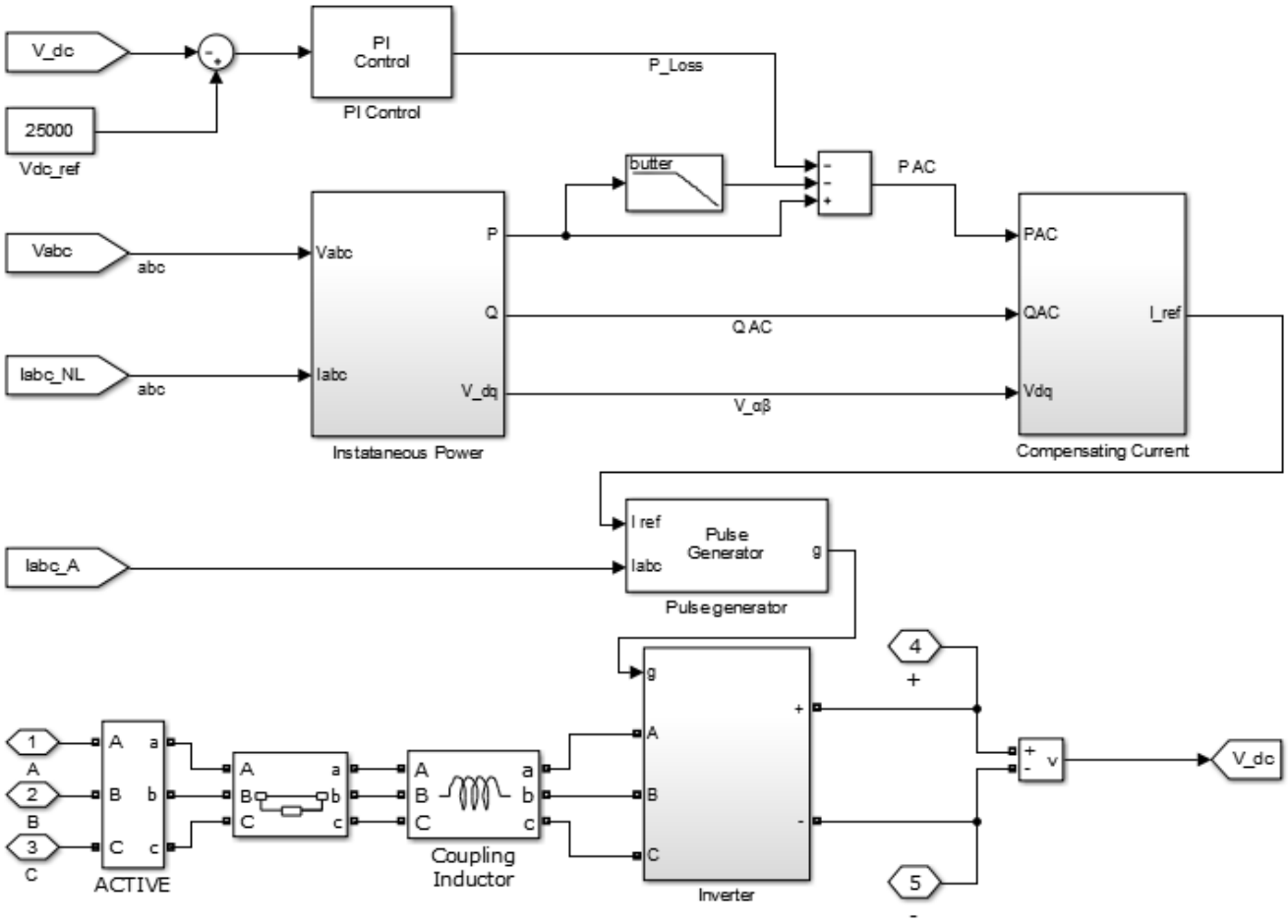

Fig. 6.3:The internal design of the SAPF block diagram.

The compensating reference current calculation in α-β frame can be determined depending on a set of equations (Eq. (3.1)-Eq.(3.4)). Which are implemented as follows:

A. Two-Phase Calculation Block

Fig. 6.4 shows the block diagram of the two-phase calculation method used to convert the three phase measurements into a two-phase model (α-β) using Clarke transformation according to Eq. (3.1).

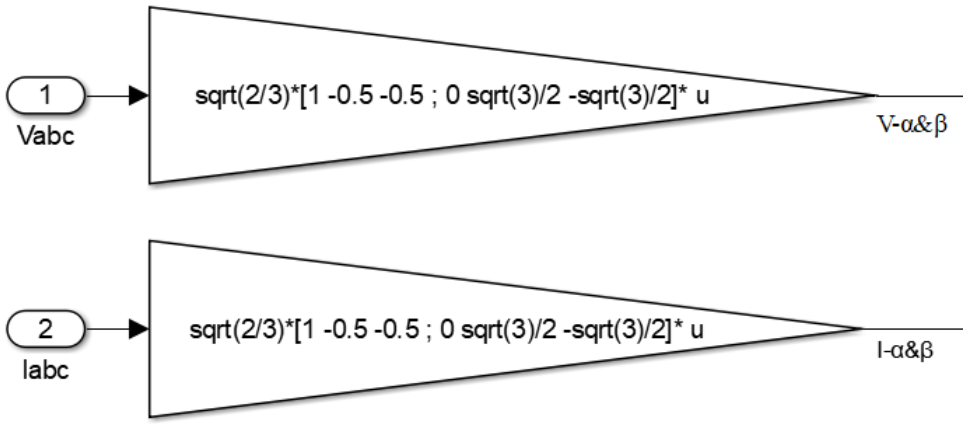

Fig. 6.4: α-β values calculation by Clarke transform

B. Instantaneous Power Calculation Block

The instantaneous reactive power calculator modelled by implementing Eq. (3.2), as shown in Fig. 6.5.

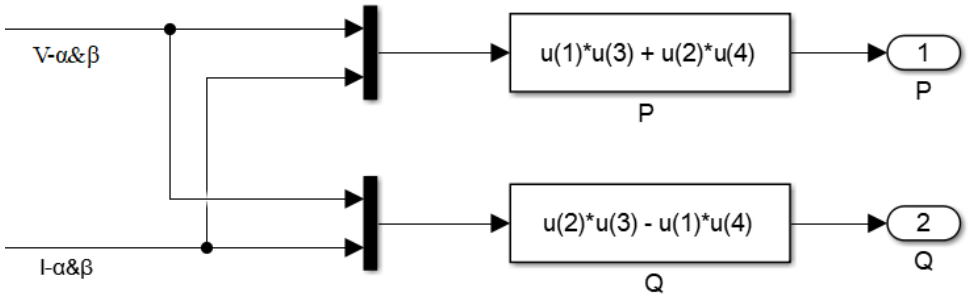

Fig. 6.5: Instantaneous power calculator block diagram

Where, u(1)=Vα, u(2)=Vβ, u(3)=Iα, u(4)=Iβ

C. Selection of the Power to be Compensated

The model for the AC real power calculation from the total power is shown in Fig. 6.6.

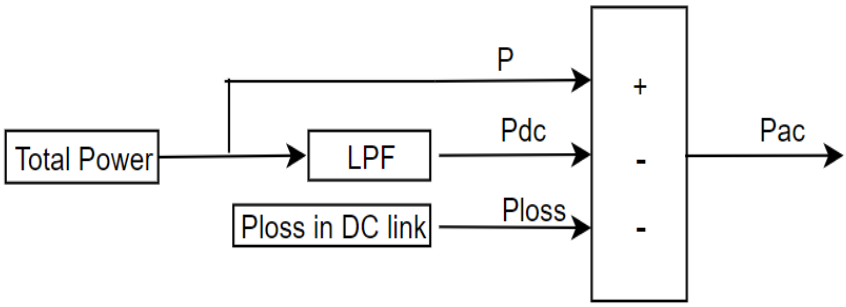

Fig. 6.6: Mechanism of selection the real power to be compensated.

D. Reference Current Calculation in α-β system

Fig. 6.7 shows the block diagram of compensating currents in two phase mode *(Iα-ref , Iβ-ref)* that can be calculated using Eq. (3.3).

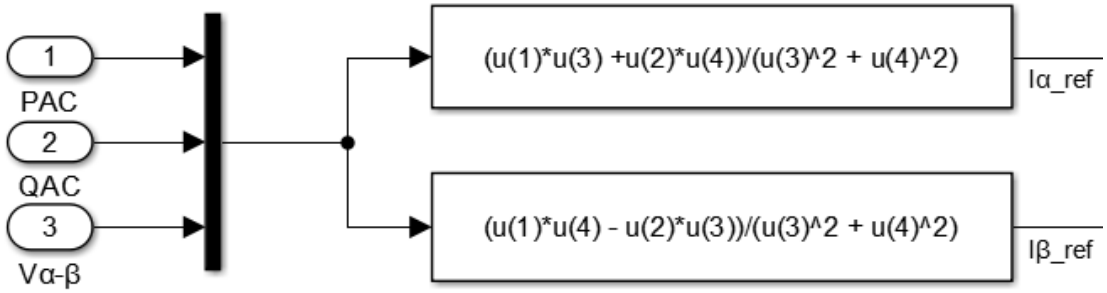

Fig.6.7: The model for reference current calculation in α-β system.

where, u(1)=P_AC, u(2)=Q_AC, u(3)=Vα, u(4)=Vβ

E. Three-Phase Reference Current Calculation Block

Compensating current in three-phase mode is mandatory for a three-phase inverter, and can be evaluated using inverse Clarke transform according to Eq. (3.4), as shown in Fig. 6.8.

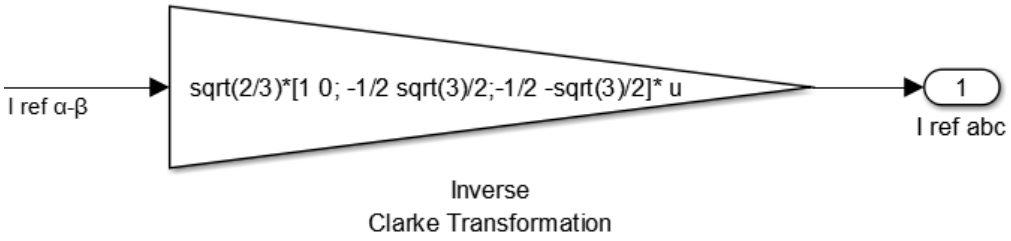

Fig. 6.8: Reference current calculation block diagram in a three-phase system.

6.3 Current Controller Model

A Hysteresis Current Controller (HCC) is implemented in the simulation model shown in Fig. 6.9. The Hysteresis Band (HB) is set to, for example, 10A in the worst case, as shown in Fig. 6.10.

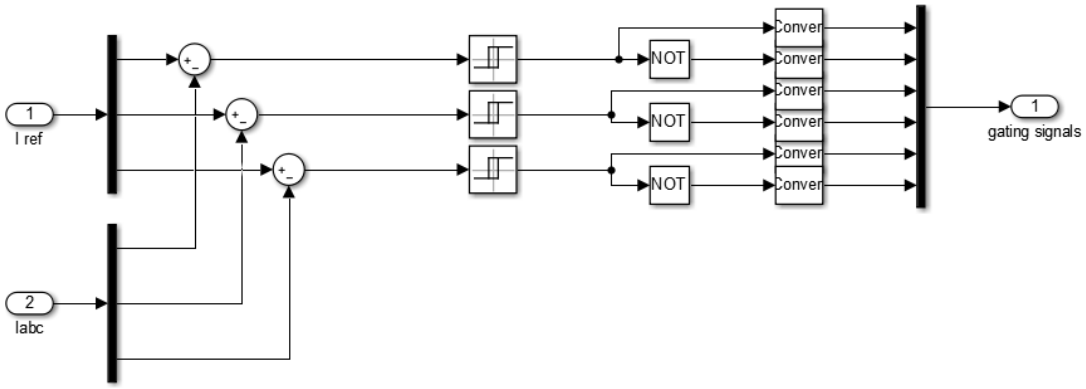

Fig. 6.9: Hysteresis Current Controller (HCC) simulation model

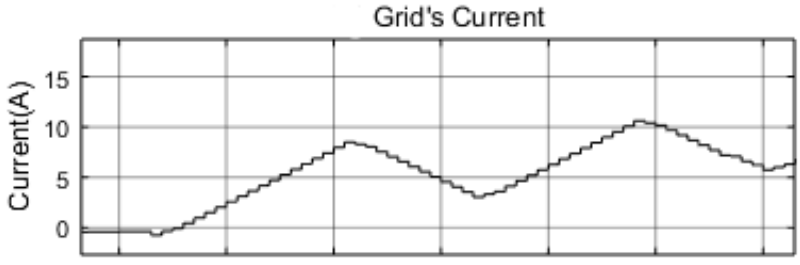

Fig. 6.10: Current ripple in a part of grid's current after inserting SAPF.

There are other current control techniques, and the most famous one is PI controller that will be discussed in simulation part, in addition to other optimization techniques such as Particle Swarm Optimization, and Genetic Algorithm.

Since one of the objectives in this thesis is to compare different topologies of SAPF, two main converters will be used; (i) Three-phase Two-level inverter, and (ii) Five-level NPC inverter.

6.4 General Results of SAPF.

The performance of SAPF system is studied in the presence of non-linear load using Matlab/Simulink. Overall simulation time is set to 1.5s, SAPF becomes active after the first five cycles (100 ms). General results obtained are as follows:

A. Instantaneous Power Calculation.

Fig. 6.11 shows a zoomed-in view of the load's real power (P_L) and the load reactive power (Q_L) calculation results. It is clear that, the real power is pulsating around it's average value, which is 3.25 MW.

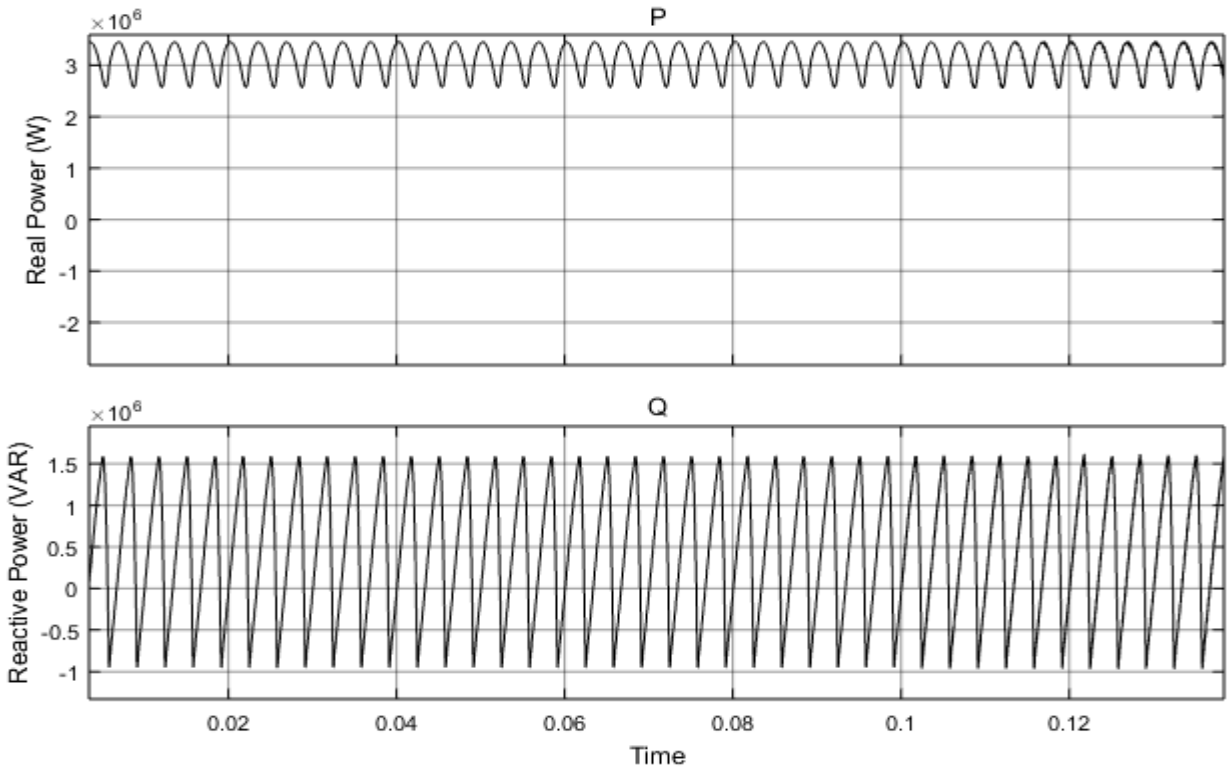

Fig. 6.11: Instantaneous real and reactive power results.

The DC (Average) power is:

$$P_L = \frac{(Vout)^2}{RL}$$

But the output voltage of load of the three-phase rectifier is:

$$\mathrm{V_{out}} = \frac{3*\sqrt{2}}{\pi} * Vrms = \frac{3*\sqrt{2}}{\pi} * 11000 = 14.855\ kV$$

Therefore,

$$P_L = \frac{(Vout)^2}{RL} = \frac{(14855)^2}{68} = 3.25\ MW$$

B. Selection of Power to be Compensated.

Fig. 6.12 shows a zoomed-in in view of the total real power consumed by the load (supplied by grid utility and other renewable energy resources); (a) total power of the load, (b) Average power ($\bar{P}$) that is consumed by the fundamental component (at 50 Hz), (c) Harmonics power ($\tilde{P}$) that is consumed by harmonics other than fundamental frequency (other than 50 Hz).

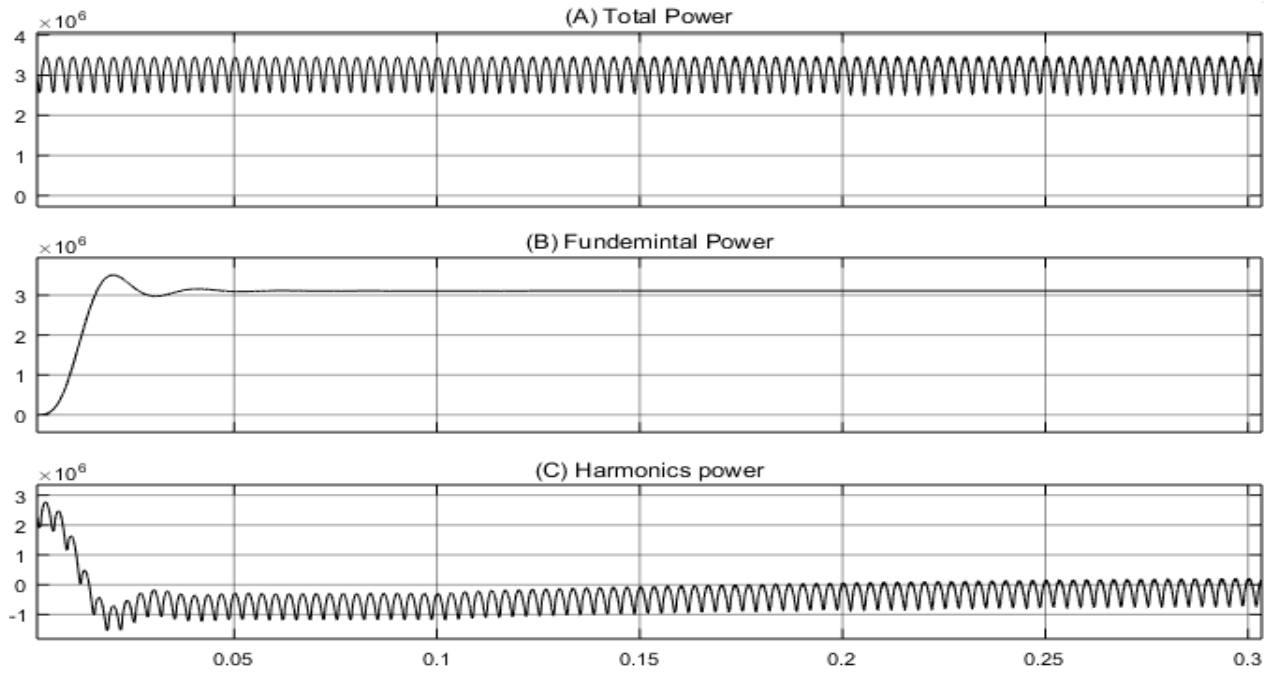

Fig. 6.12: Real power waveforms; (a) total consumed power, (b) power consumed by 50 Hz component, (c) Power consumed by other harmonics

It is clear that, the total power is composed of two components; $\bar{P}$ and $\tilde{P}$; $\tilde{P}$ must be inverted as the purpose of using SAPF is generating the same of grid harmonics, but in opposite direction.

C. *Three-Phase Reference Current Calculation.*

Generating three-phase reference currents depends on evaluating the reference currents in the α-β model according to eq. (3.3) followed by inverse Clarke transform according to Eq. (3.4) to get the references for the three-phase model. Fig. 6.13 shows a zoomed-in view of reference current waveforms in a three-phase model (supplied by SAPF).

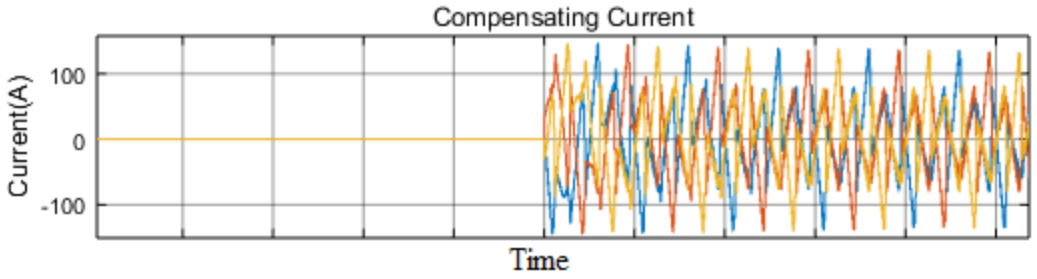

Fig. 6.13: Reference current signals of three-phase model.

D. Overall System Performance.

Fig. 6.14 and Table. IV shows SAPF performance before and after inserting SAPF to the utility grid. The SAPF implements a two-level inverter. Fig. 6.15 shows a zoomed-in view of the waveforms of Fig. 6.14.

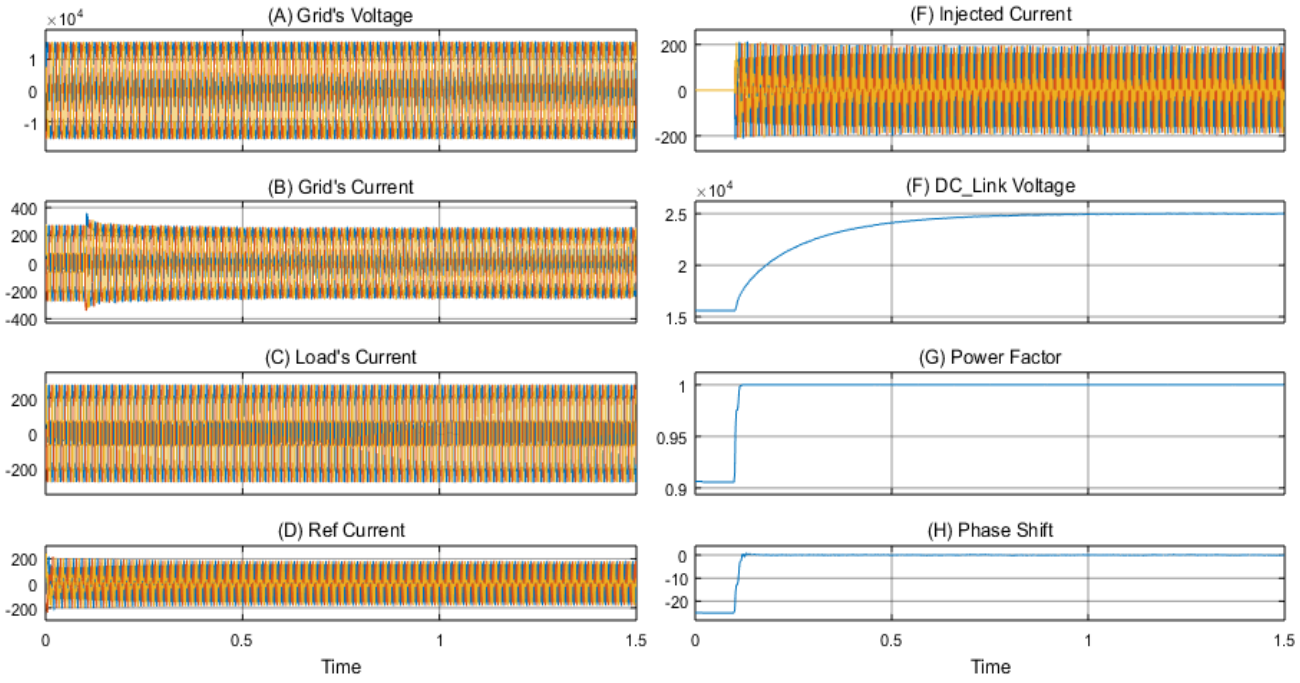

Fig. 6.14: Shunt-APF performance; (A) Grid's Voltages waveforms, (B) Grid's Current waveforms, (C) Load's Currents' waveforms, (D) Reference Currents' waveforms, (E) SAPF Injected Currents' waveforms, (F) DC-Link charging curve, (G) Combined Power Factor and (H) Phase Shift regulation curve

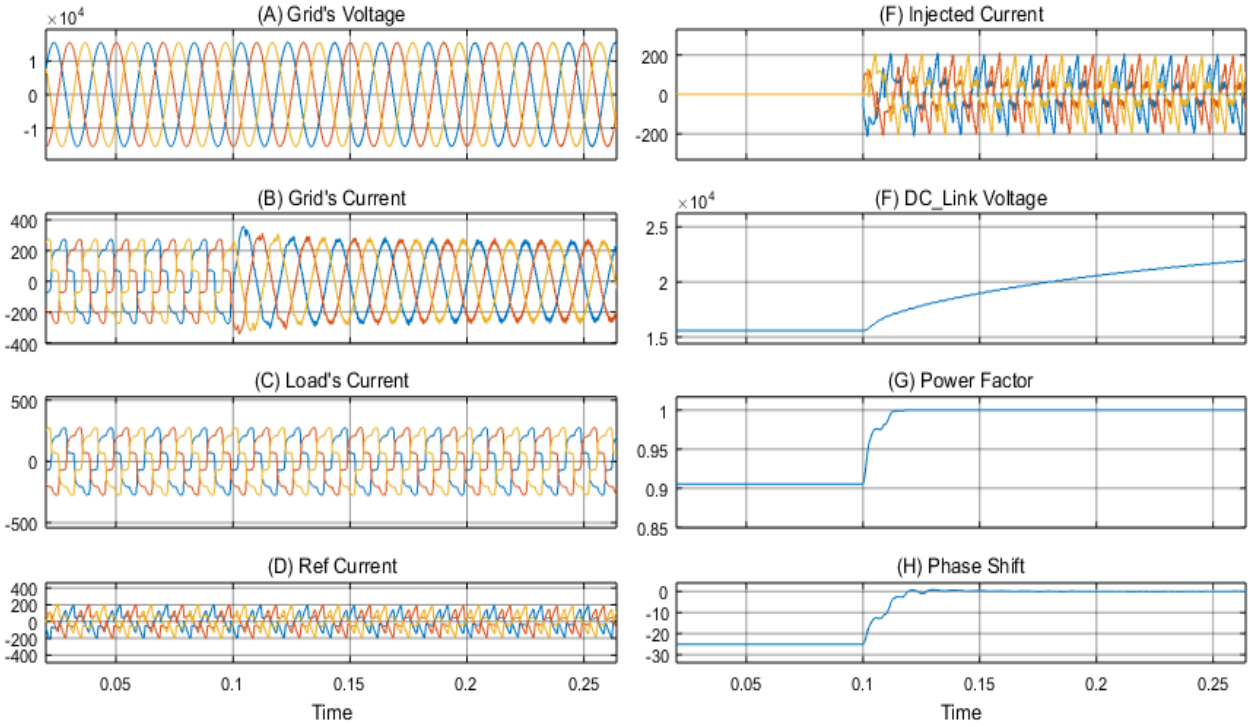

Fig. 6.15: Zoomed-in view of the waveforms of the SAPF showing its performance; (A) Grid's Voltages waveforms, (B) Grid's Current waveforms, (C) Load's Currents' waveforms, (D) Reference Currents' waveforms, (E) SAPF Injected Currents' waveforms, (F) DC-Link charging curve, (G) Combined Power Factor and (H) Phase Shift regulation curve

Table IV: Grid's performance before and after adding the SAPF.

Comparison of	**Before adding SAPF**	**After adding SAPF**
THD_i [%], without a smoothing capacitor for load	24	4.1
THD_i [%], with a smoothing capacitor for load (100uF)	51.8	3.9
PF	0.9	1

Fig. 6.16 shows THD[%] reduction over the operating period before and after inserting the SAPF in presence of a smoothing capacitor across the tested load; AC/DC rectifier load with a smoothing capacitor. It is clear that, the SAPF reduces the THD[%] from 51.8% to 3.9%.

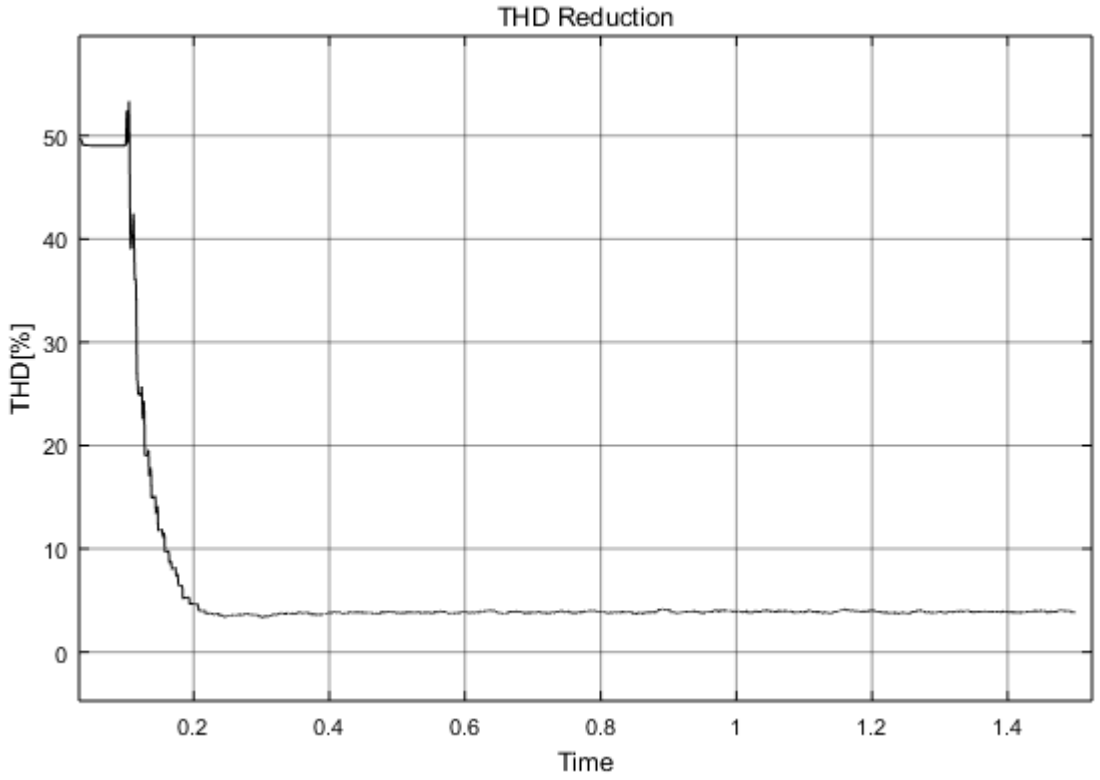

Fig. 6.16: The THD[%] is reduced when the SAPF was inserted across the nonlinear load at t=0.1s.

Fig. 6.17 shows FFT analysis of grids current before and after inserting SAPF, it is clear that grid's current full of wide range of harmonics (odd and even) before inserting SAPF while all of this distortion disappears after installing proposed SAPF.

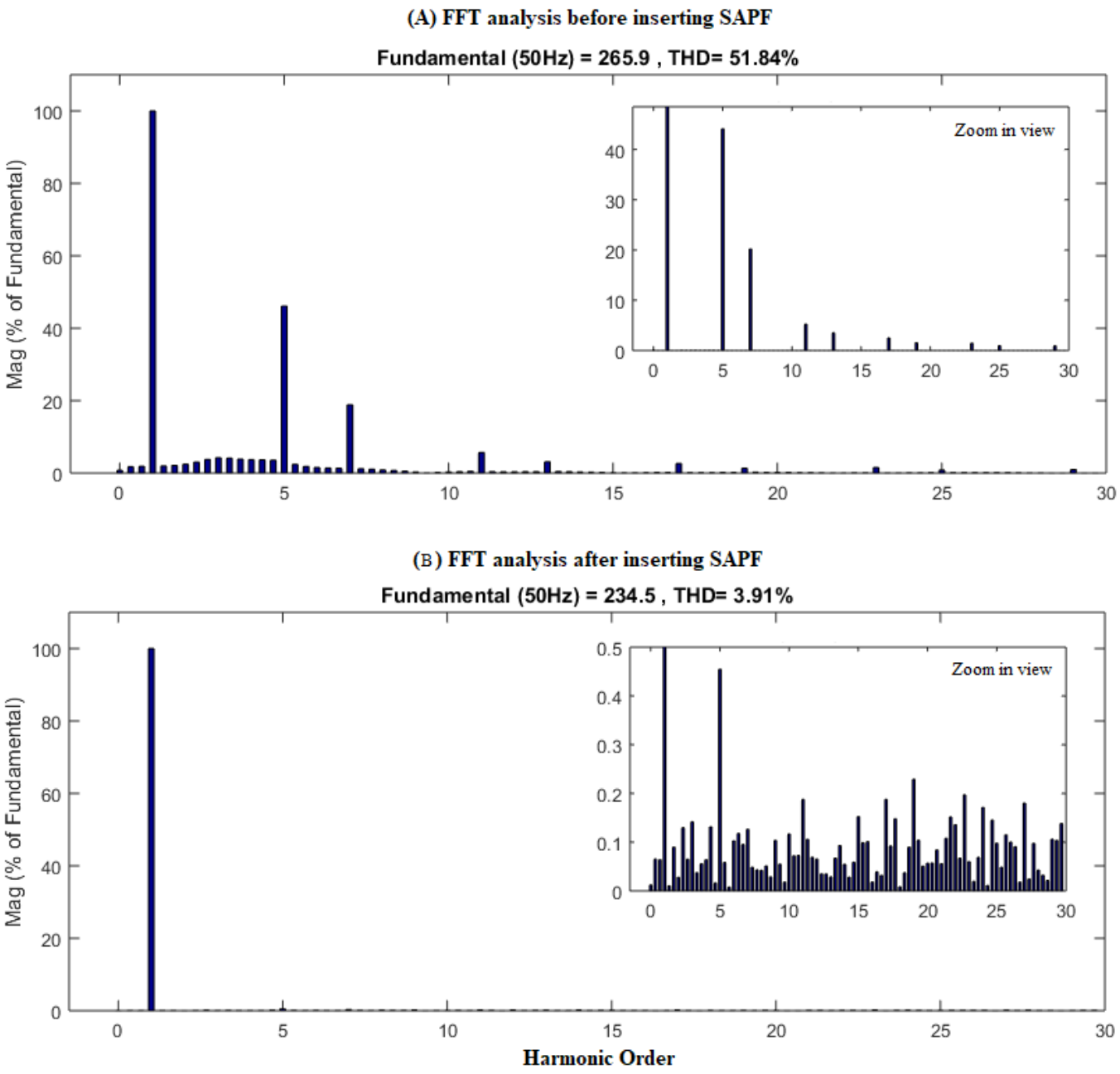

Fig. 6.17: FFT analysis of grid's current before and after inserting SAPF.

6.5 Two Level Vs Multilevel SAPF

Two-level and Multilevel SAPF's have the same performance in terms of harmonic reduction. Fig. 6.18 and Fig. 6.19 shows the SAPF performance with Two-level and Multilevel, respectively, with the same environmental andsimulation conditions. Table. V compares between Two-level and Multilevel SAPF in terms of THD.

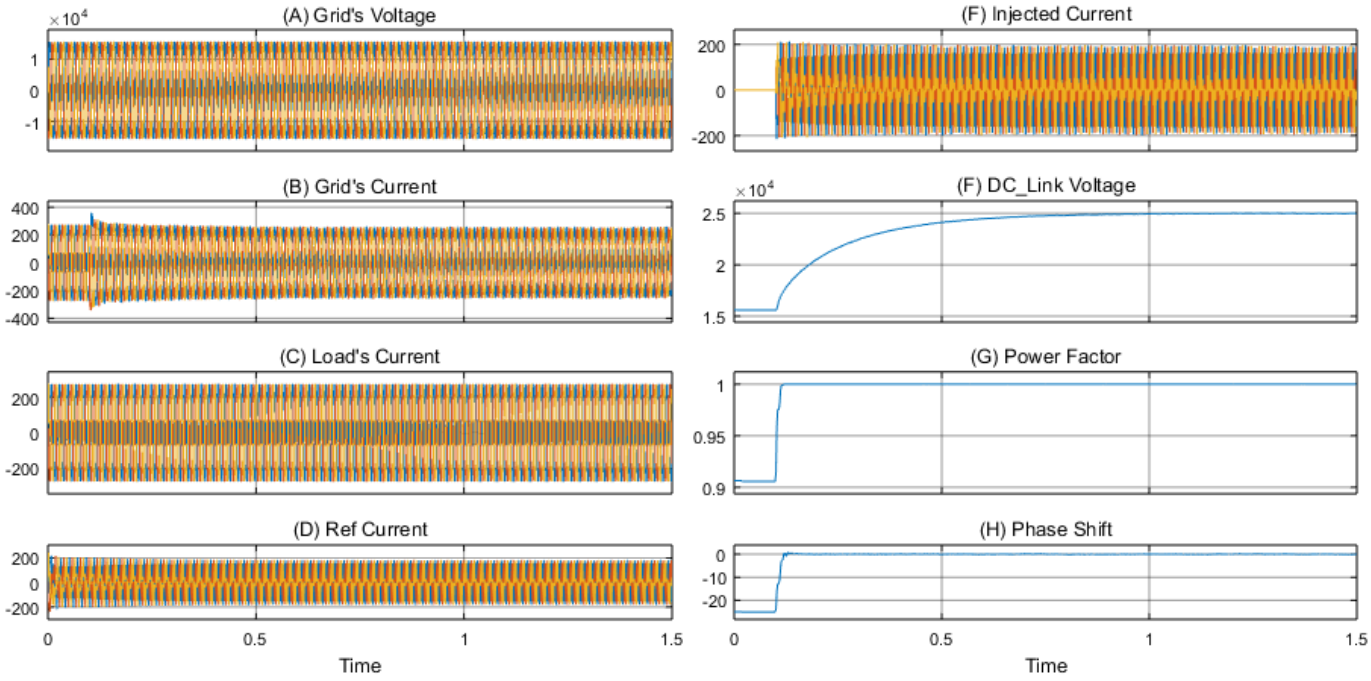

Fig. 6.18: The SAPF performance with Two-level inverter; (A) Grid's Voltages waveforms, (B) Grid's Current waveforms, (C) Load's Currents' waveforms, (D) Reference Currents' waveforms, (E) SAPF Injected Currents' waveforms, (F) DC-Link charging curve, (G) Combined Power Factor and (H) Phase Shift regulation curve

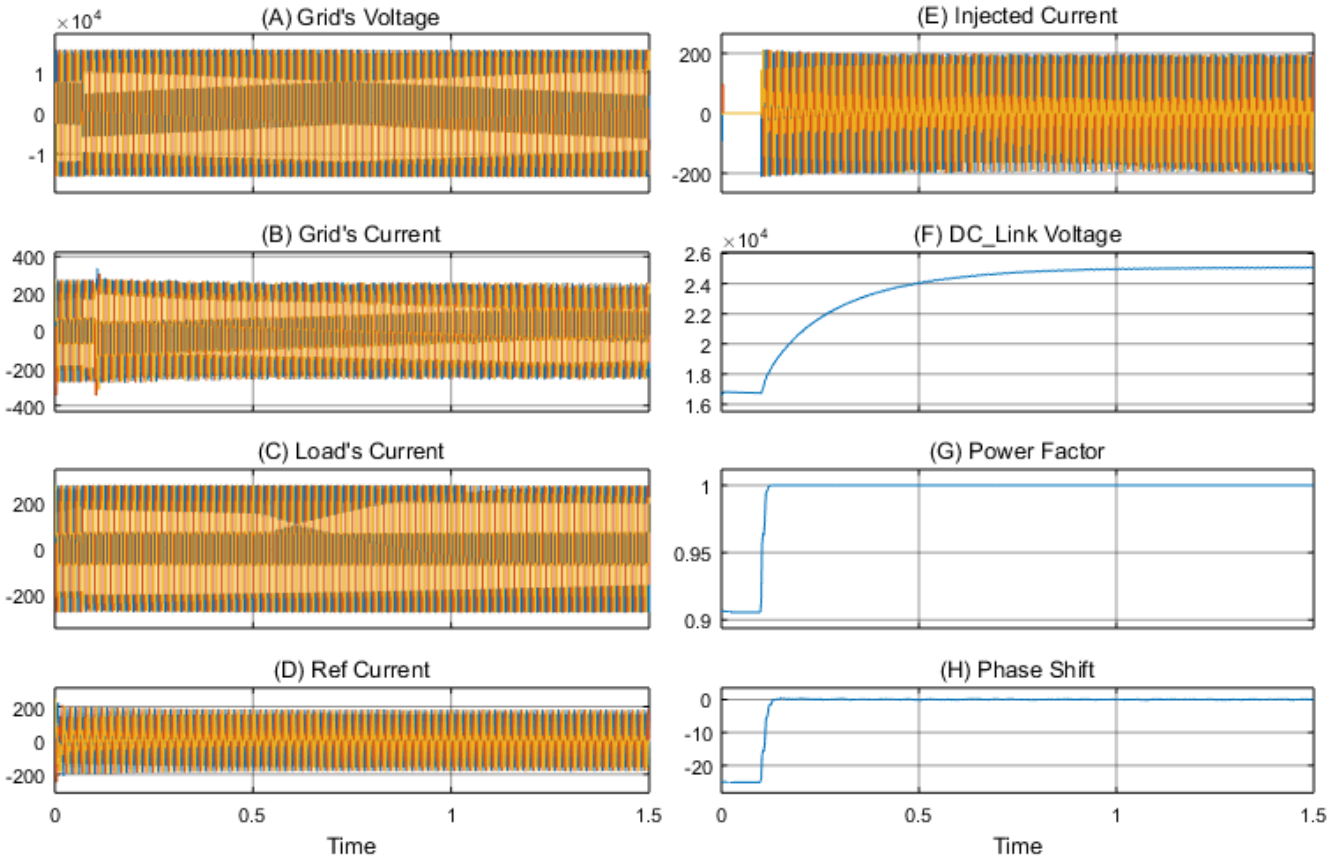

Fig. 6.19: SAPF performance with Multilevel inverter; (A) Grid's Voltages waveforms, (B) Grid's Current waveforms, (C) Load's Currents' waveforms, (D) Reference Currents' waveforms, (E) SAPF Injected Currents' waveforms, (F) DC-Link charging curve, (G) Combined Power Factor and (H) Phase Shift regulation curve

Table V: Two level and Multilevel SAPF comparison in terms of harmonic reduction.

Comparison of	Before adding SAPF	After adding SAPF
THD_i [%] of Two-level SAPF	24	4.1
THD_i [%] of Multilevel SAPF	24	2.7

It's clear that, multilevel SAPF gives lower THD with the same switching frequency of two-level SAPF. In practice, two level inverter cannot be used in medium voltage applications, since it has low voltage blocking of its IGBTs (IGBT factories produce switches up to 6.5KV till now [53]). Fig.6.20 shows why Two-level SAPF is not suitable, while Five level SAPF is suitable for MV applications (11KV case).

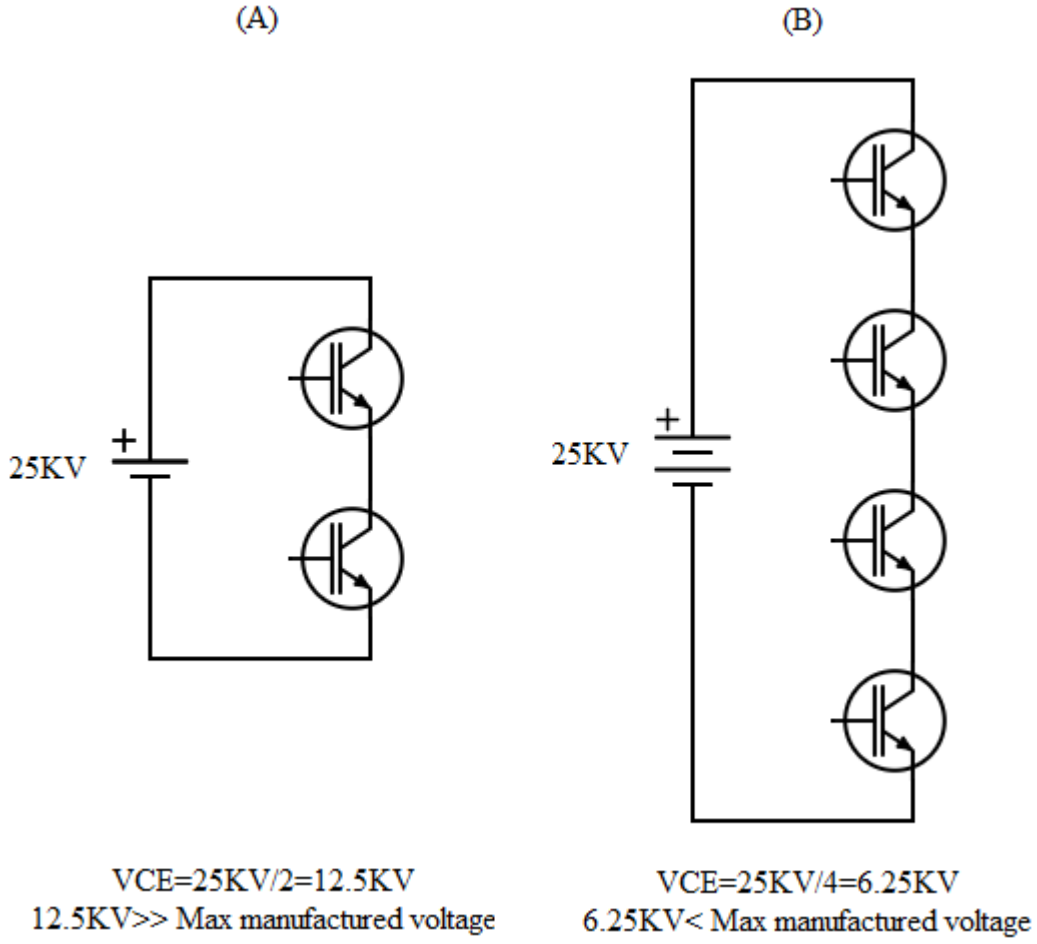

Fig. 6.20: DC-Link voltage distribution on bridge switches; (A) Two-level SAPF, (B) Multilevel SAPF.

6.6 ***Hysteresis vs PI Controller of SAPF***

Hysteresis Current Controllers (HCC), Double Band Hysteresis Current Controllers (DBHCC), and PI controllers are the main controllers used for harmonic compensation in SAPF. Fig. 6.21 shows a zoomed-in view of grid's current after inserting SAPF for used controllers. Table. VI compares between the three types of controllers in terms of THD reduction.

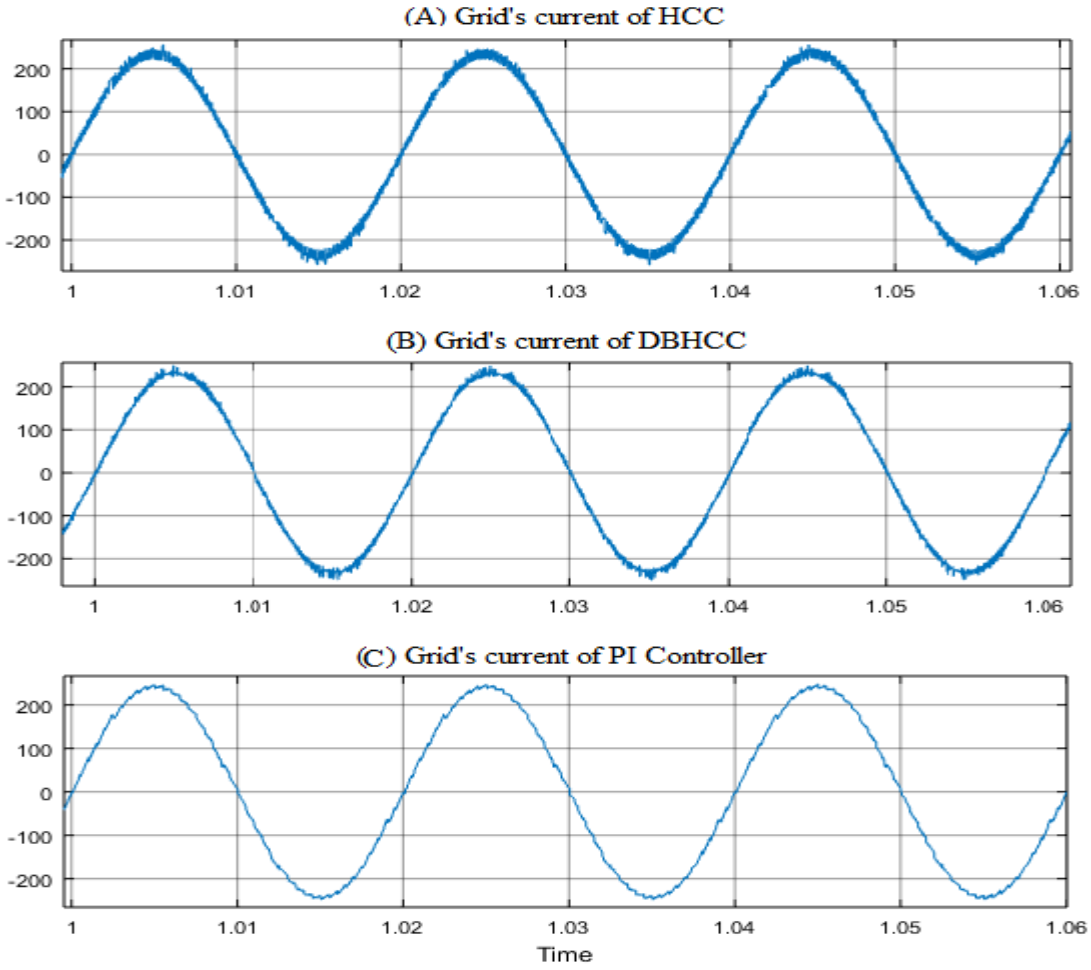

Fig. 6.21: Grid's current waveforms after inserting SAPF implementing; (A) HCC, (B) DBHCC, and (C) PI Controller.

Table VI: HCC and PI controllers comparison in terms of harmonic reduction.

Comparison of	**Before adding SAPF**	**After adding SAPF**
THD_i [%] implementing HCC	24	4.2
THD_i [%] implementing DBHCC	24	2.8
THD_i [%]implementing PI	24	19

It is clear that, implementing a DBHCC gives lower THD with lower switching losses. Anyway, PI controllers gives the best THD and losses reduction.

In general, the performance of a hysteresis controller depends on its hysteresis band. For example, a narrow hysteresis band can give very low THD in comparison with a PI controllers, but with very high switching losses. The main drawback of HCC is it's uncontrollable switching frequency, which means that it's switching frequency is not fixed and it may be high enough to damage switching devices by adding significant switching losses, while that does not occur in a PI controller.

6.7 ***Adaptive Power Factor in SAPF***

Achieving a unity power factor is one of the main purposes of SAPF, but that is not needed all the time. Some applications need lead or lag power factor to be adapted, such as power factor compensation of nearby loads, as was shown previously in Fig. 5.1. Fig. 6.22 shows adapting power factor from 0.9 lag to 0.9 lead.

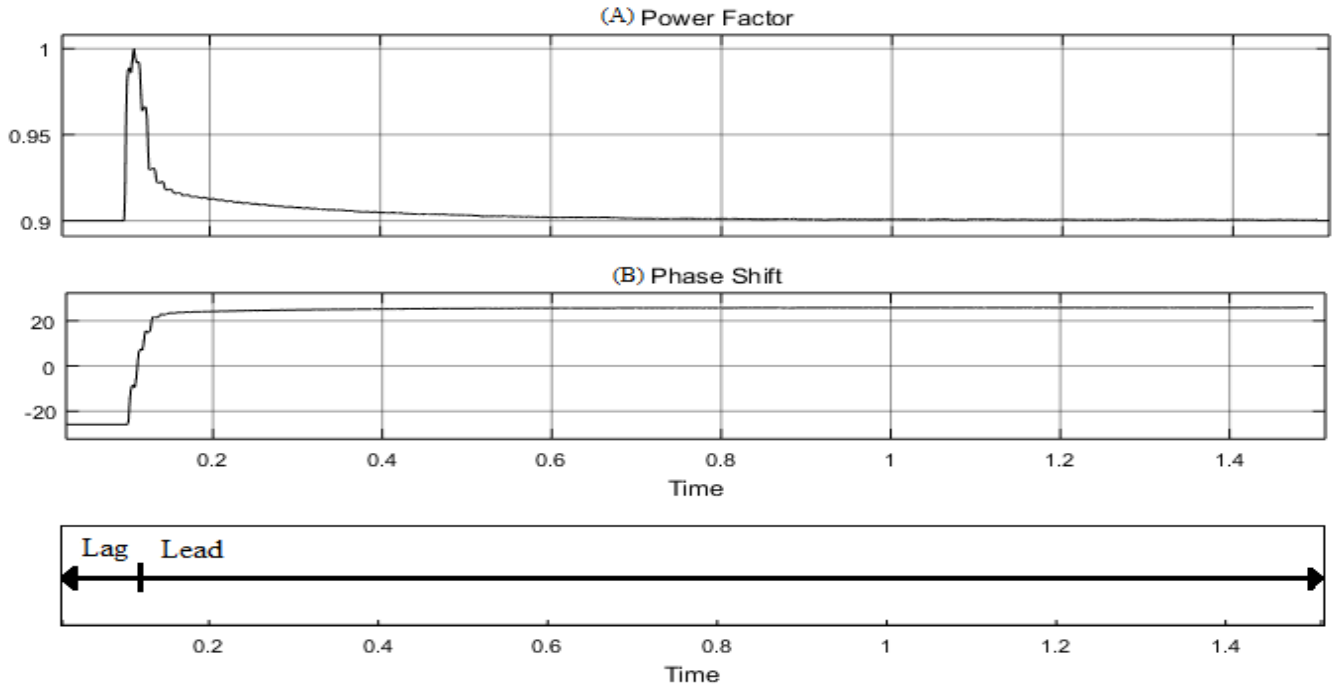

Fig.6.22: Adaptive Power Factor from 0.9 lag to 0.9 lead.

It's clear that, the SAPF can be used as a flexible device to adapt power factor smoothly to avoid any transient that may occur by traditional capacitor banks in addition to its ability to be adapted at a target power factor accurately without steps.

6.8 ***Adaptive DC_Link Voltage***

Adaptive DC_Link voltage, based on voltage regulation of DC bus, depends on a set of equations that was discussed previously in section 4.1.3. Fig. 6.23 shows how the DC bus voltage varies when sag and swell events occur in a utility grid. Fig. 6.24 shows how the DC bus voltage is regulated by varying the connected load and increasing it up to twice that of the connected load. Fig. 6.25 shows adaptive DC bus voltage behavior during fault conditions.

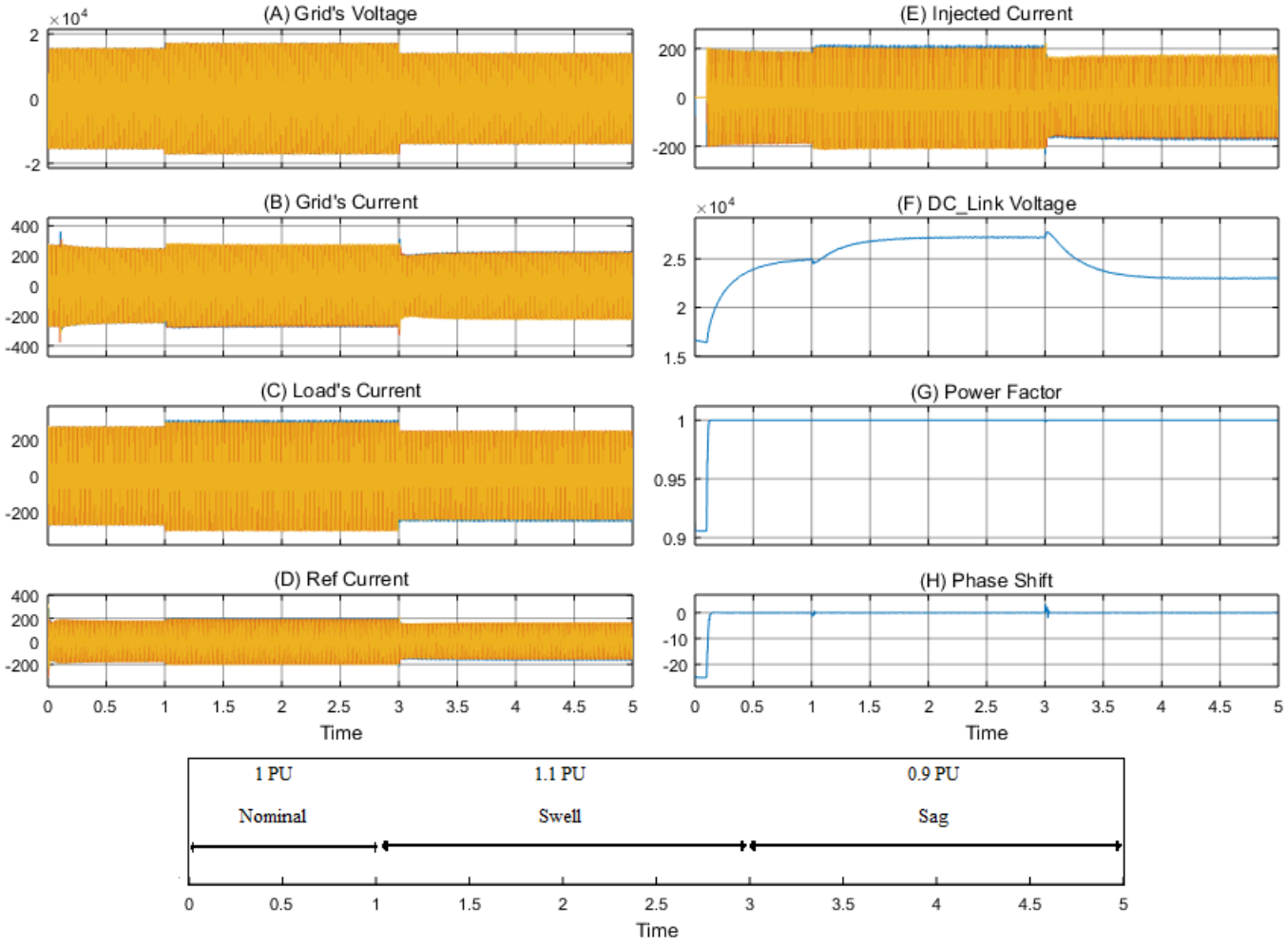

Fig. 6.23: Variation of the DC bus voltage when sag and swell events occur in the utility grid

It's clear that DC_link voltage adapted to meet the voltage variation of utility grid (sag and swell events), and that's in order to increase the SAPF dynamic response against voltage variations. Sag limitation within range of [0.75-1] PU to work properly. When sag event exceeds 25%, the DC-link voltage is reduced beyond the minimum allowable value (18.18 KV) and SAPF will not work correctly.

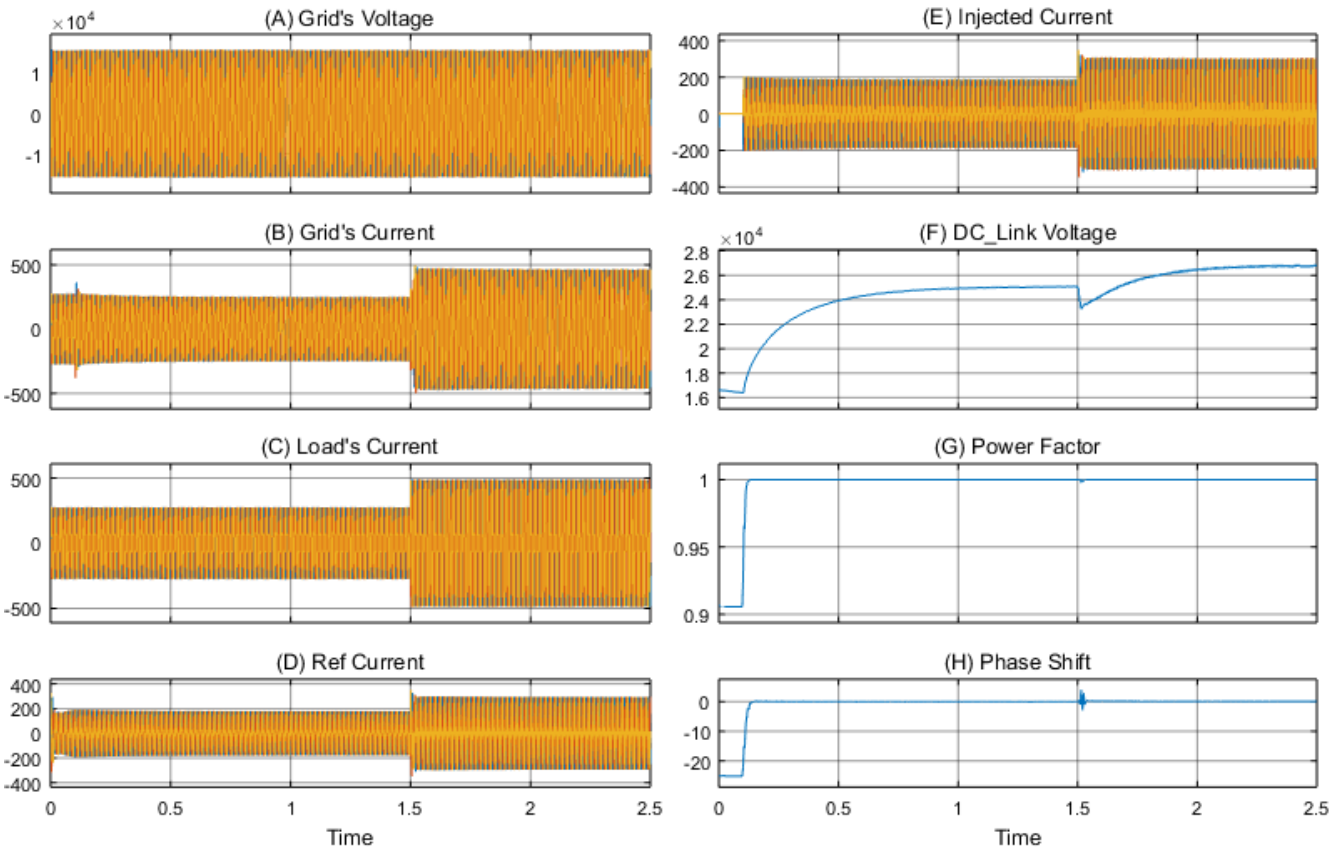

Fig. 6.24: DC bus voltage regulated by varying the connected load and increasing it up to twice the value of the connected load.

It's clear that, the DC_Link voltage is adapted automatically depending on a set of equations (Eq. 4.3 – Eq. 4.8). At the moment of 1.5s, the load increases up to twice of its value, and the DC_link voltage also increased in order to keep THD at the same level before 1.5s moment, and that increases the dynamic response of the SAPF against load variations (keep THD level constant with load variations).

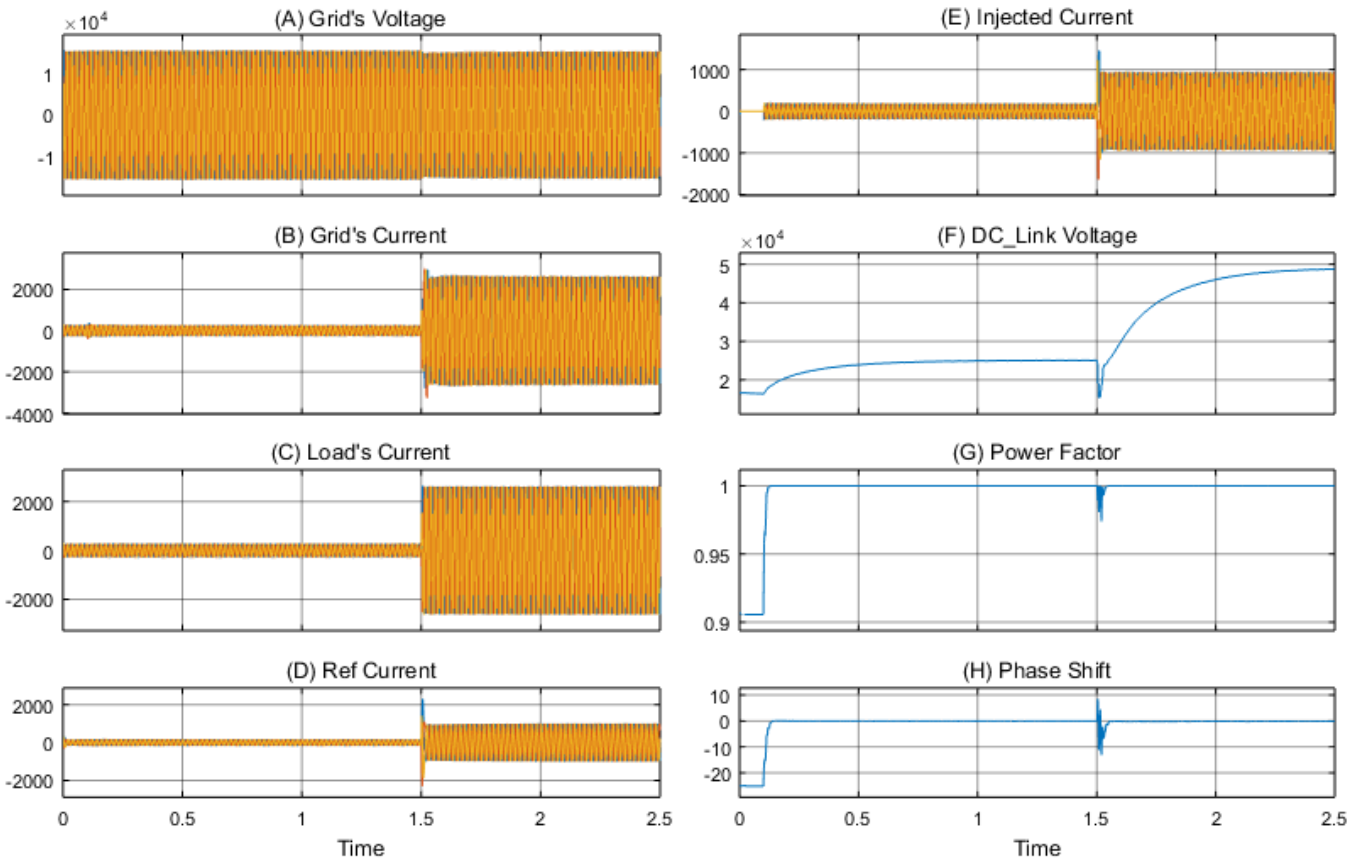

Fig. 6.25: Adaptive DC bus voltage behavior in fault conditions (Symmetrical Fault).

It's clear that, the main drawback of adaptive voltage method is its behavior during faults conditions, faults increasing the injected current and that leads to increasing the DC bus voltage in uncontrollable manner, which means that this overvoltage will damage switching devices.

Adaptive DC_Link method first proposed by Rida Musa in [30]. Musa tested the proposed adaptive method during sag and swell conditions only, and his results confirm the results in this thesis, as shown in Fig. 6.23 above, the same proposed method was tested during other scenarios:

- Load variation condition: the proposed method has a good dynamic response to load variation.
- Fault condition: it is the main drawback of this method, faults establish an overvoltage on the DC bus that may damage switching devices. Section 6.9 will address this problem and design protection system to obtain safe operation of SAPF in all conditions.

6.9: SAPF Protection System

This section addresses the design of a protection system for the SAPF in order to increase its safe operation during different transient cases such as; (i) overload, (ii) fault and (iii) inrush current.

6.9.1: Overload Protection

Fig. 6.26 shows the ability of the current limiter in protecting the SAPF from overload condition by clipping the peak of the injected current when it exceeds the designed value (500A).

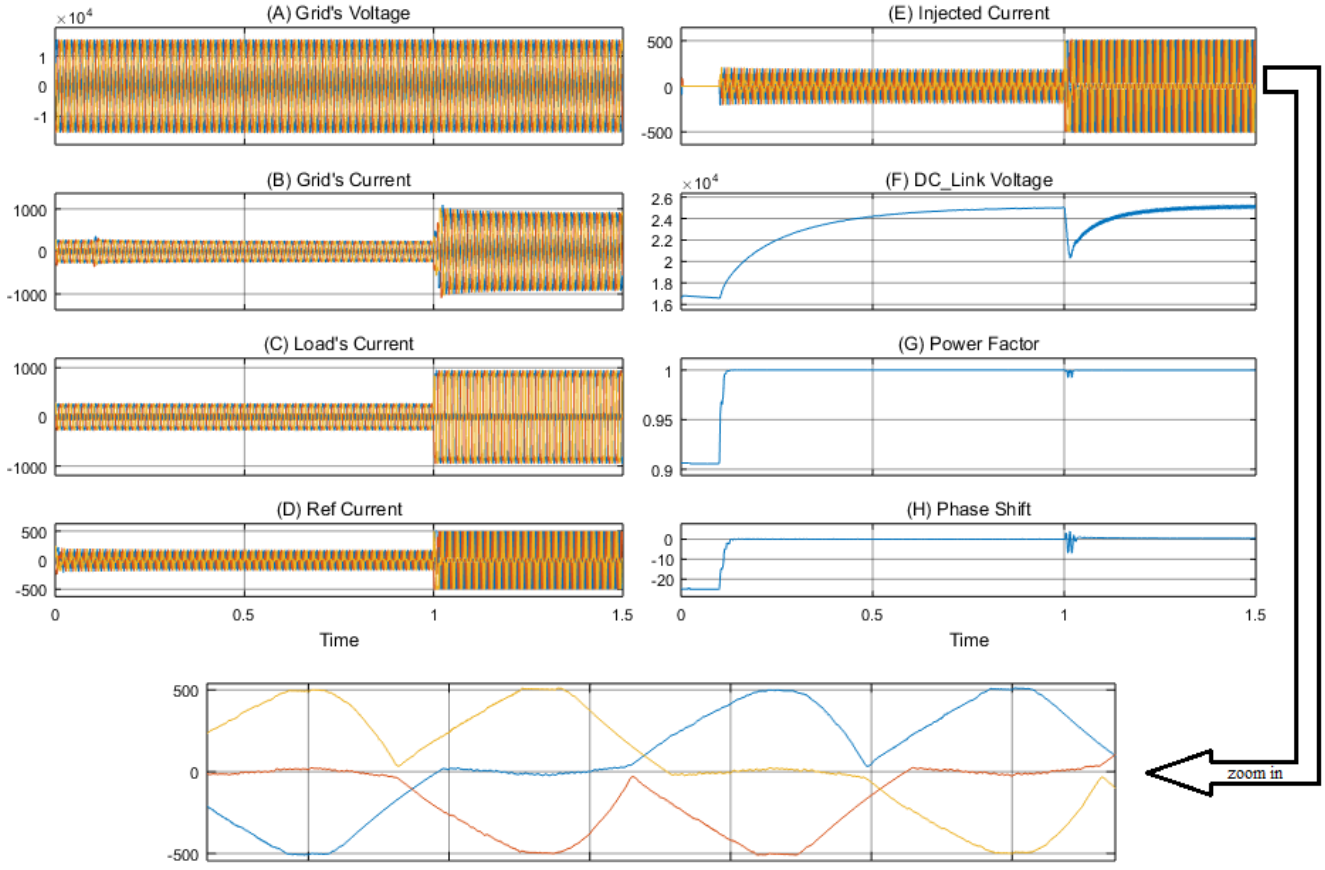

Fig. 6.26: The Current limiter performance in the SAPF protection from overload condition by clipping the peak current from exceeding the designed value (500A).

It's noted that, the SAPF clipping peak current from exceeding the maximum designed value (500A) in order to protect IGBTs from being overloaded and/or damaged.

6.9.2: Fault Protection

Fig. 6.27 shows the performance of the SAPF protection system during a fault condition by interrupting both the DC_Link inside the inverter and AC switch at PCC.

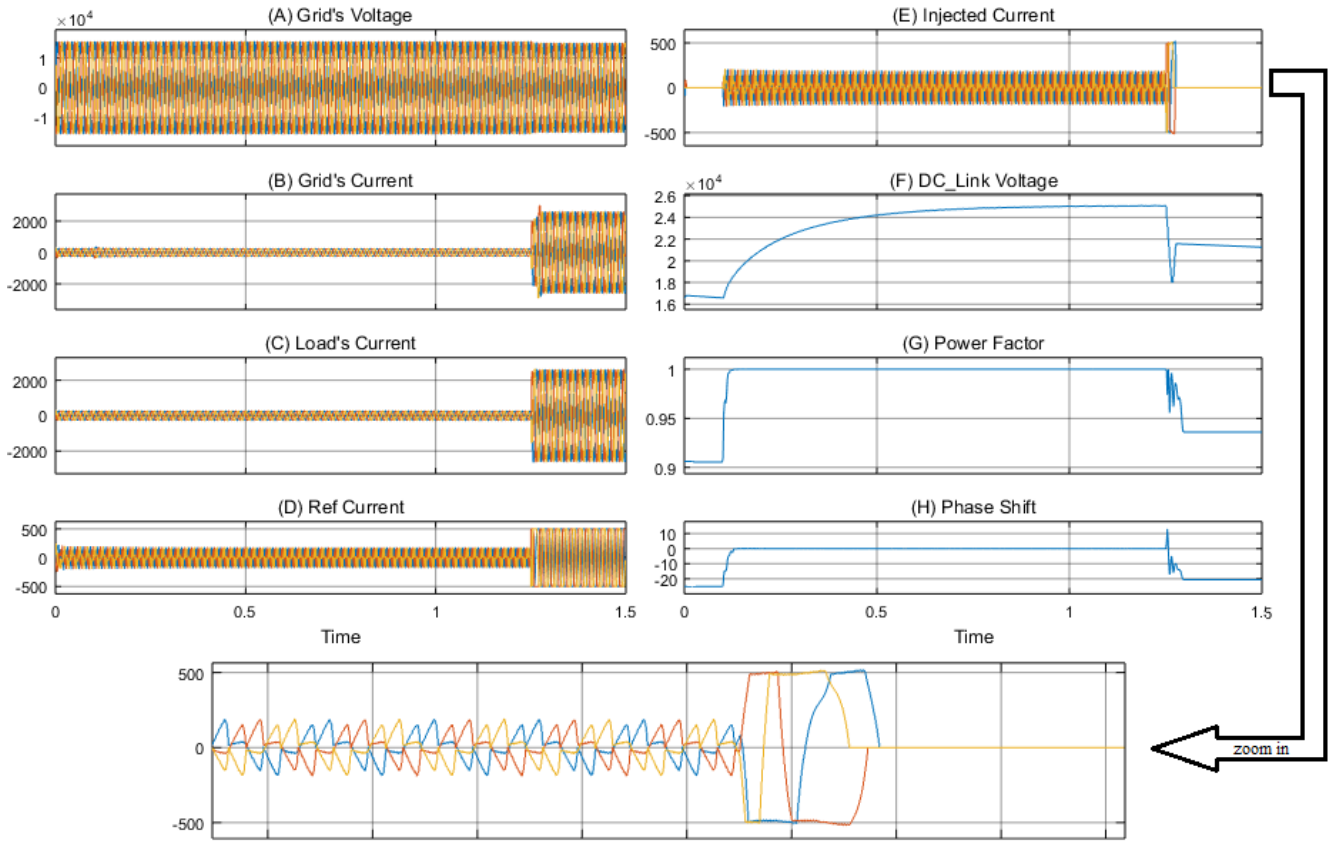

Fig. 6.27: Performance of SAPF protection during fault conditions

It is clear that, the proposed protection system protects the SAPF from overcurrent that occurs during fault conditions with fast response (within one cycle, 20ms), in addition to clipping the injected current to the maximum designed value (500A) in order to protect the SAPF during the fault moment.

6.9.3: Inrush Current Protection

Fig. 6.28 shows the SAPF performance during energizing a distribution transformer (the inrush current) in parallel with non-linear load. Fig 6.29 shows the same waveforms with a zoomed-in view.

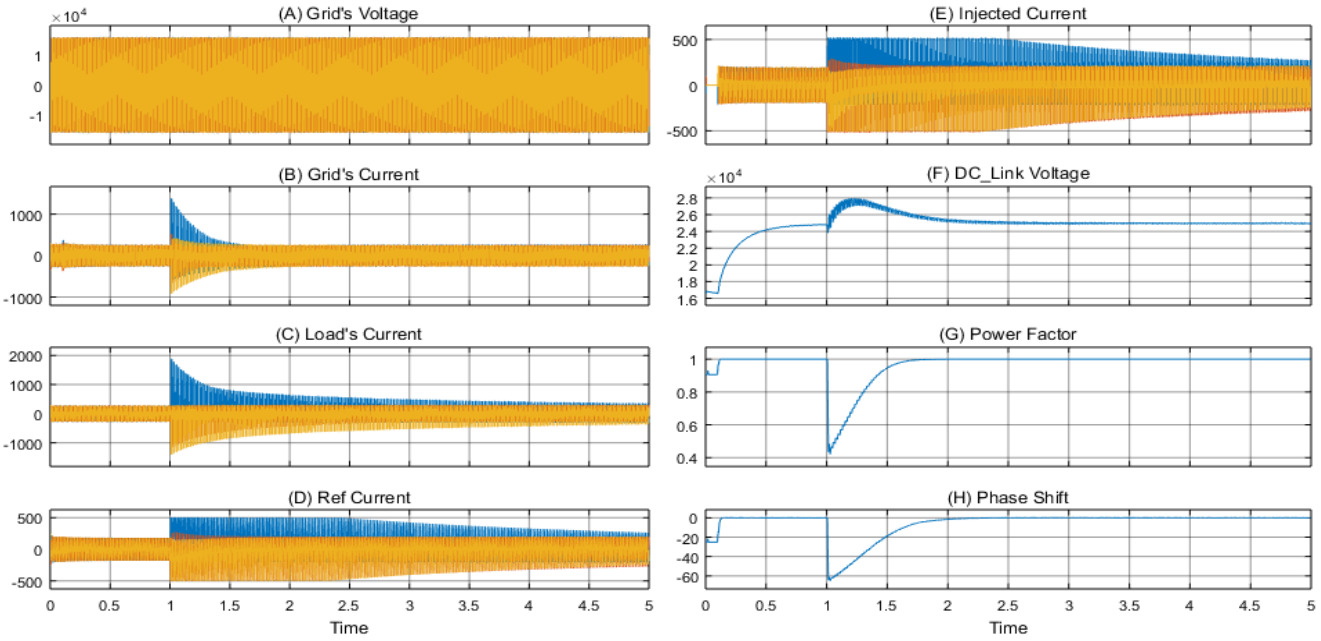

Fig. 6.28: The SAPF performance during energizing a distribution transformer (the inrush current)

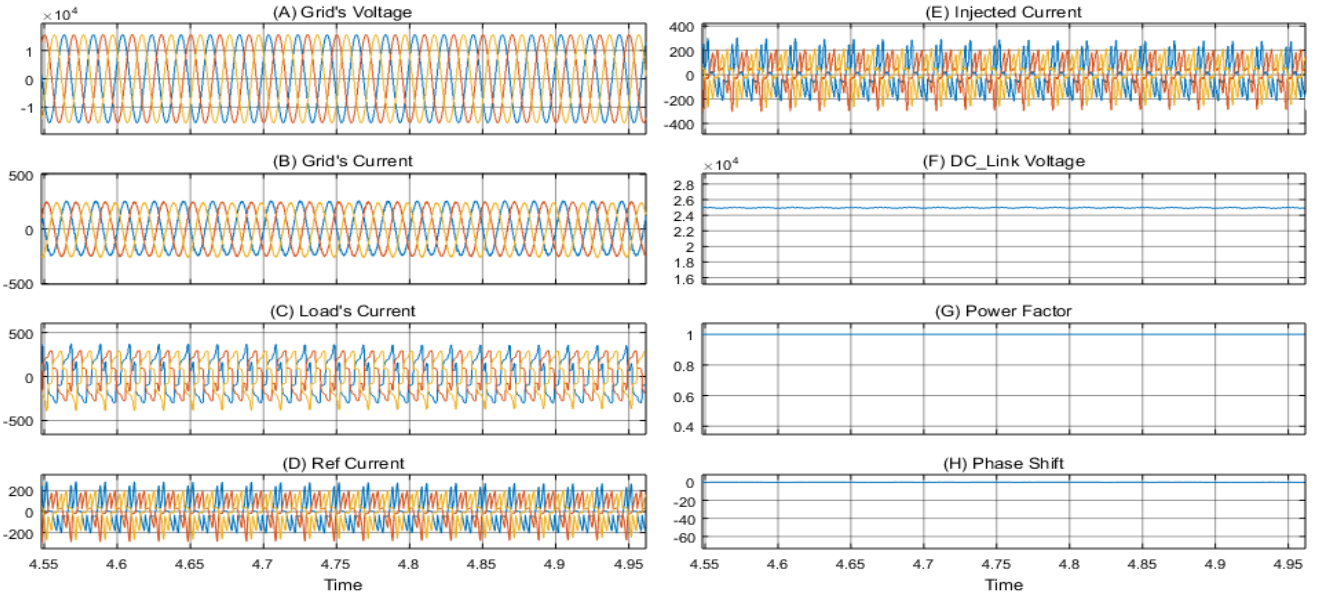

Fig. 6.29: A zoomed-in view of the SAPF waveforms during energizing a distribution transformer, with compensating harmonic distortion feature

It is clear that, the designed protection system can make a discrimination between fault and inrush current; it disconnects the CB during the fault case, while still in operation during inrush current case implementing second harmonic ratio method. The SAPF is suitable for reducing the inrush current effect by decreasing the inrush current amplitude and decreasing its period up to 15% of the normal inrush condition as classified in 6.28 (B) and 6.28 (C), the main side effect of using SAPF as inrush limiter is its overcharge that occurs across its DC-Link during inrush period.

6.10 Case Study for SAPF

This section studies the SAPF performance of an actual MV grid harmonic distortion in Hebron city as a part of HEPCO utility grid. Fig. 6.30 shows a single line diagram (SLD) of the selected feeder. Fig. 6.31 shows an FFT analysis barograph collected by data logger device. Fig. 6.32 shows the current waveforms of selected feeder. Table VII shows the collected harmonic distortion of a MV switchgear feeder.

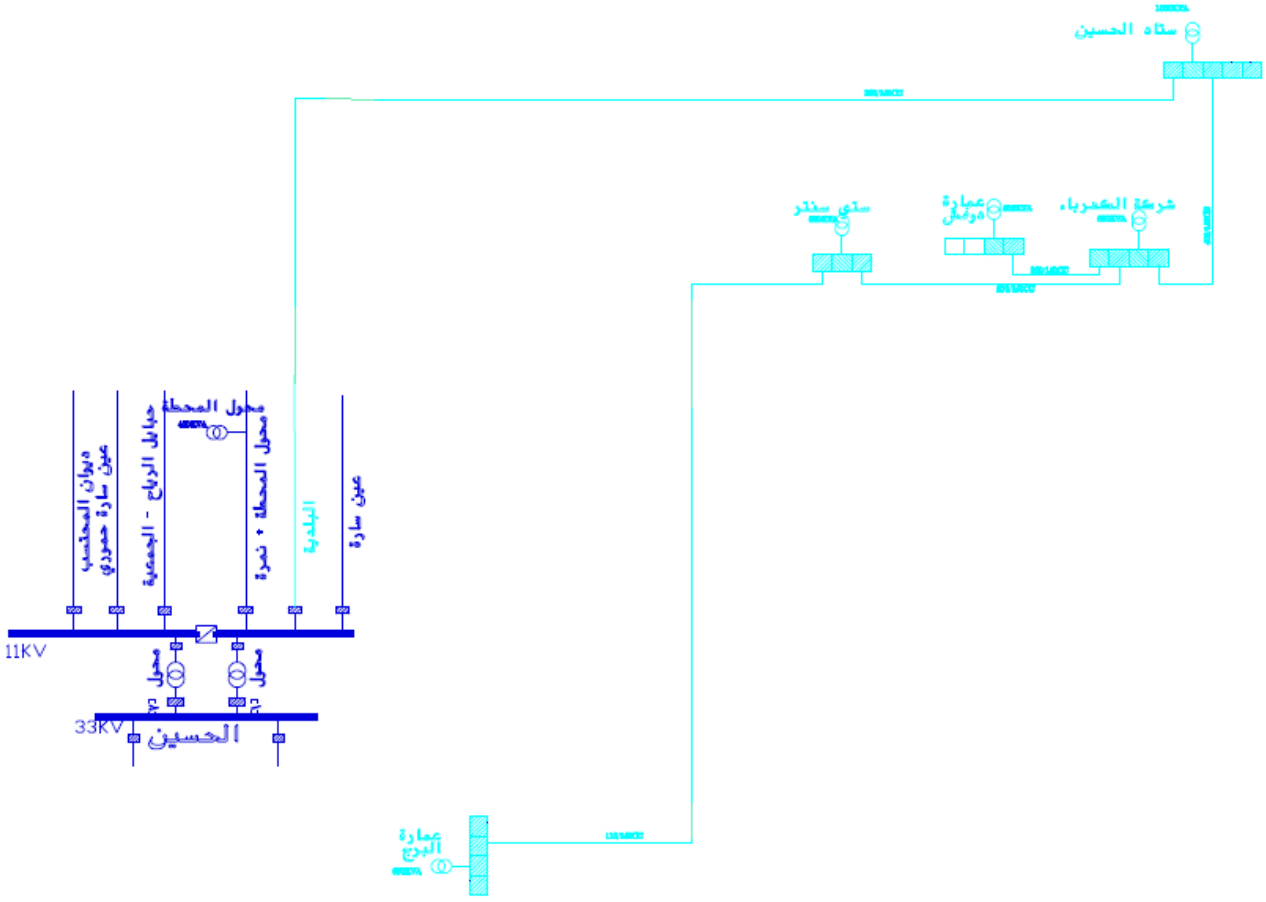

Fig. 6.30: Selected substation and feeder of the case study.

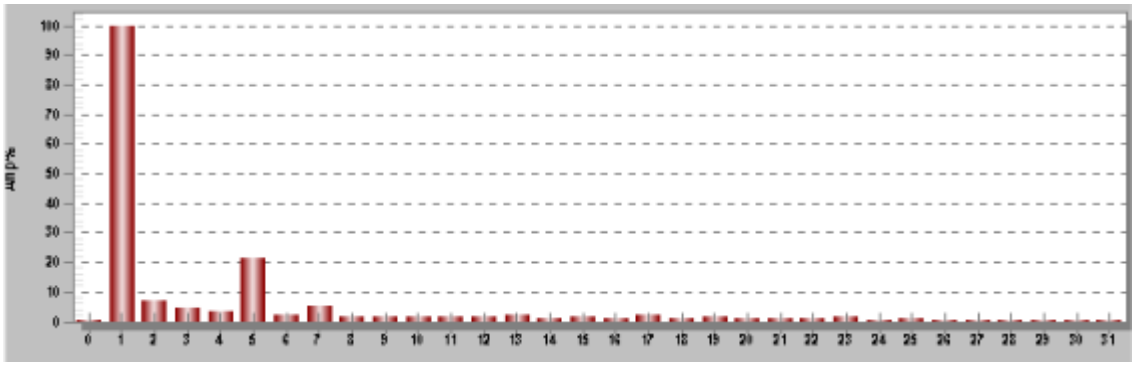

Fig. 6.31: FFT analysis barograph collected by data logger device (DENT device).

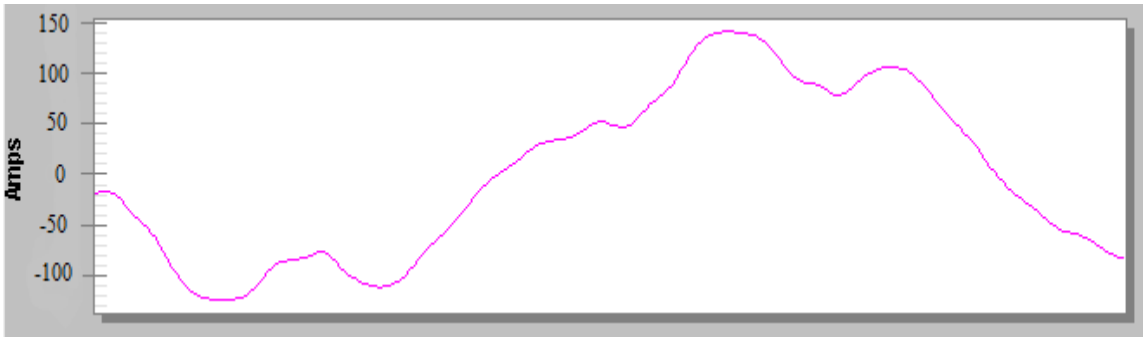

Fig. 6.32: Current waveform of selected feeder taken by data logger (DENT device).

Table. VII: Current harmonic distortion contents of the selected feeder

Harmonic Order	Harmonic Contents (A)
1	95.6
2	7
3	4.8
4	3.4
5	16.5
6	2.3
7	4.9
8	1.7

9	1.6
10	1.4
11	1.7
12	1.1
13	1.4
14	0.9
15	0.9
16	0.8
17	2.8
18	0.8
19	1.6
20	0.6
21	0.7
22	0.6
23	0.8
24	0.6
25	0.5
26	0.5
27	0.5
28	0.5
29	0.4
30	0.5
31	0.5
THD [%]	**19.8%**
K-Factor	**5.3**

The collected data was programmed via MATLAB /Simulink by implementing each harmonic content as individual current source (31 current sources at different frequencies). Fig. 6.33 shows the performance of SAPF when installed and implemented in a real case study. Fig. 6.34 shows the same waveforms of Fig. 6.33 with a zoomed in view. Table VIII shows a comparison before and after installing the SAPF with the real case study in terms of THD and PF.

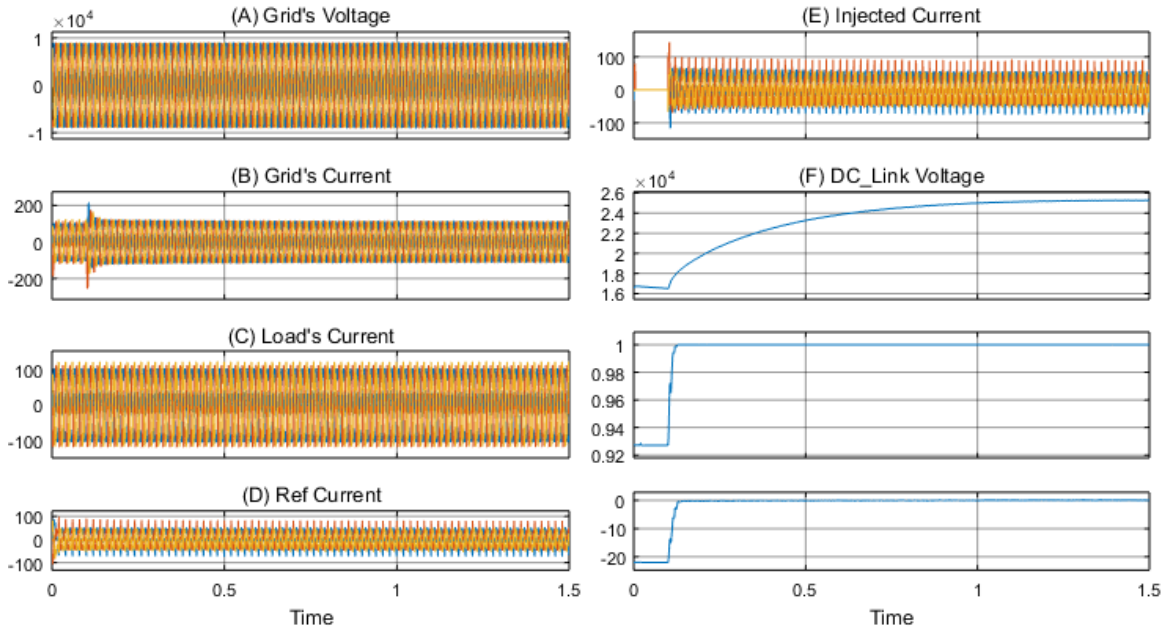

Fig. 6.33: The SAPF performance when implemented in the real case study

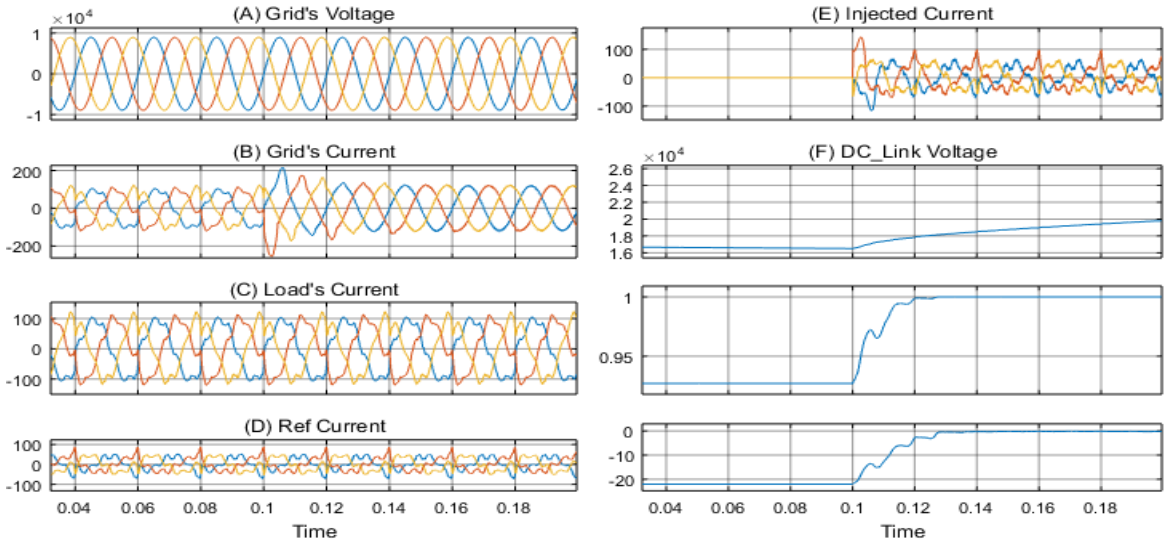

Fig. 6.34: SAPF performance when implemented in a real case study (zoomed-in view).

Table VIII: SAPF performance comparison before and after installing it with case study.

Comparison of	Before adding SAPF	After adding SAPF
THD_i [%]	19.8	3
PF	0.92	1

It is clear that, the proposed MV SAPF operates properly with an actual utility grid. Simulation shows that, the SAPF achieves both goals of harmonic reduction and PF correction. Fig. 6.35 shows FFT analysis before and after connecting the SAPF.

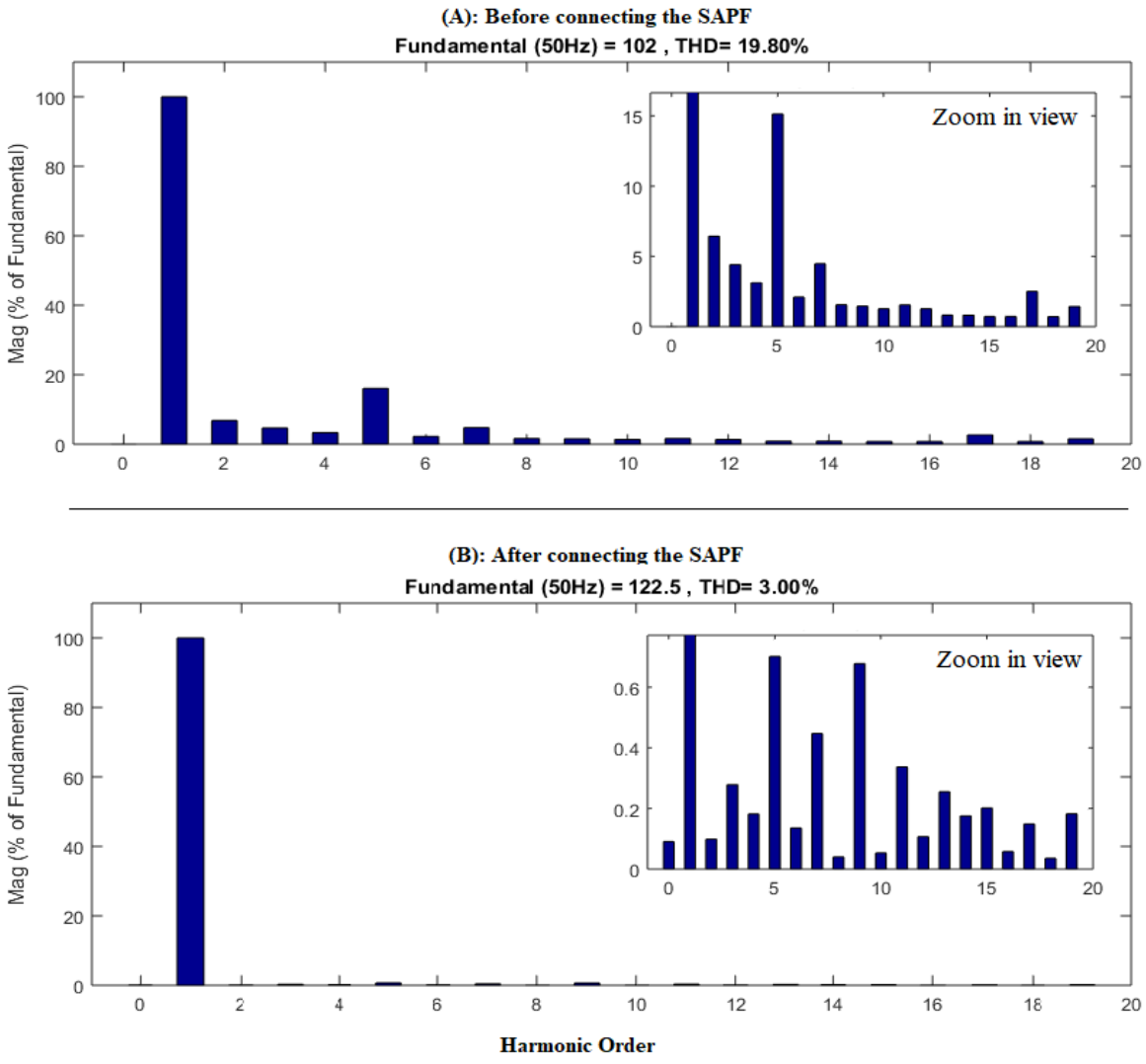

Fig. 6.35: FFT analysis of utility current, (A): before connecting the SAPF, (B): After connecting the SAPF.

Chapter Seven

Conclusions and Future Work

7.1 Conclusions

This thesis studied SAPF design, performance and it's safe operation in MV networks with non-linear loads that draw high contents of current harmonics. Different types of inverters, Two-level inverter and Multilevel NPC inverter, were studied implementing one of the main types of the control techniques; (i) HCC and (ii) PI controller. This study shows that, the Multilevel SAPF gives lower THD than the Two-level SAPF, and more suitable in MV applications, since it has a lower voltage stress on its inverter's IGBTs. Besides, the study shows that the PI controller is better than HCC in terms of THD reduction under the same conditions, and that leads to decreasing the value of the coupling inductor and its losses.

Adaptive power factor is a new application of SAPF replacing the well-known application (unity power factor), and that's very useful to supply nearby loads prior the PCC of the SAPF with reactive power. Adaptive DC-Link voltage is also new method in recent publications as mentioned previously. It gives a better dynamic response to grid variation in comparison with fixed DC-Link voltage, while it has a bad response during fault conditions.

Safe operation of SAPF is also studied in order to develop a protection system against transient conditions such as; (i) Overload, (b) Fault and (c) Inrush current. The proposed protection system is based on digital current limiter to avoid switchs damage in addition to implementing second harmonic ratio to make a discrimination between fault and inrush current.

Finally, this thesis studied a practical case of HEPCO utility grid by measuring current harmonic components at site, then implementing it as a load parallel to the proposed SAPF. Simulation shows that, the proposed SAPF operates properly for both of harmonic reduction and power factor correction purposes in this practical case.

7.2 Future Work

Future work of this thesis may focus on two main orientations:

A. Using SAPF in Renewable Energy (RE) applications by implementing PV source as input of the DC-Link of SAPF.

B. Developing an auto-tuned PI controllers using optimization techniques.

C. Implement SAPF and its control scheme using the Microlab box present at Birzeit University Labs.

References

[1] A. Baggini. *Handbook of power quality*. John Wiley & Sons, 2008.

[2] Singh, Mukhtiar, et al. "Grid interconnection of renewable energy sources at the distribution level with power-quality improvement features." *IEEE transactions on power delivery* 26.1, pp. 307-315, 2011.

[3] B. Singh. K. Al-Haddad and A. Chandra, "A Review of Active Filters for Power Quality Improvement," *International IEEE Transactions on Industrial Electronics*. Vol. 46. No. 5, pp. 960-971, October 1999.

[4] H. Akagi, "New Trends in Active Filters for Power Conditioning", *IEEE Transactions on Industry Applications*, vol. 32, no. 6, pp. 1312-1322, Nov./Dec. 1996.

[5] José Rodríguez,Jih-Sheng Lai, And Fang ZhengPeng, " Multilevel Inverters: A Survey Of Topologies, Controls, and Applications", *IEEE Transactions On Industrial Electronics*, Vol. 49, No. 4, August 2002.

[6] S. K. Khadem, M. Basu, and M. F. Conlon, "Power Quality in Grid connected Renewable Energy Systems: Role of Custom Power Devices*", in Proc. of Inter. Conf. on Renewable Energies and Power Quality (ICREPQ'10)*, 23-35 March, 2010, Granada, Spain.

[7] E. Pouresmaeil, D. Montesinos-Miracle, O. Gomis-Bellmunt, A. Sudria-Andreu, "Instantaneous Active and Reactive Current Control Technique of Shunt Active Power Filter Based on the Three-level NPC Inverter", *Eur. Trans. Elect. Power*, vol. 21, no. 7, pp. 2007-2022, Oct. 2011.

[8] Moftah, M. Amin, G. El-Saady, and A. Ibrahim. "Active Power Filter for Power Quality Enhancement of Photovoltaic Renewable Energy Systems." *Smart Grid (SASG), 2016 Saudi Arabia*. IEEE, 2016.

[9] Sundaram, Elango, and M. Venugopal. "On Design and Implementation of Three Phase Three Level Shunt Active Power Filter for Harmonic Reduction Using Synchronous Reference Frame Theory." *International Journal of Electrical Power & Energy Systems* 81: 40-47, 2016.

[10] T. Dao, B. T. Phung and T. Blackburn, "Effects of voltage harmonics on distribution transformer losses", *2015 IEEE PES Asia-Pacific Power and Energy Engineering Conference (APPEEC)*, pp. 1-5, 2015.

[11] C. Lombard, and A. P. J. Rens, "Evaluation of system losses due to harmonics in medium voltage distribution networks." *Energy Conference (ENERGYCON), 2016 IEEE International*. IEEE, 2016.

[12] Blooming, Thomas M., and Daniel J. Carnovale. "Application of IEEE Std 519-1992 harmonic limits." *Pulp and Paper Industry Technical Conference, 2006. Conference Record of Annual*. IEEE, 2006.

[13] Akagi, Hirofumi. "Modern active filters and traditional passive filters." *Bulletin of the polish academy of sciences technical sciences* 54.3, 2006.

[14] R. N. Beres, X. Wang, M. Liserre, F. Blaabjerg, C. L. Bak, "A review of passive power filters for three-phase grid connected voltage-source converters", *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 4, no. 1, pp. 54-69, Mar. 2016.

[15] El-Habrouk, M. K. Darwish and P. Mehta. "Active power filters: A review." *IEE Proceedings-Electric Power Applications*147.5, pp. 403-413, 2000.

[16] M. Routimo, M. Salo, H. Tuusa, "Comparison of voltage-source and current-source shunt active power filters", *IEEE Trans. Power Electron.*, vol. 22, no. 2, pp. 636-643, Mar. 2007.

[17] A. Farshid, "*Double-Band hysteresis current control method for three-phase shunt active power filters*", Diss. Eastern Mediterranean University (EMU)-Doğu Akdeniz Üniversitesi (DAÜ), 2013.

[18] H. Komurcugil, "Double-band hysteresis current-controlled single-phase shunt active filter for switching frequency mitigation", *Electr. Power Energy Syst.*, vol. 69, pp. 131-140, 2015.

[19] Q. Liu, L. Peng, Y. Kang, S. Tang, D. Wu, and Y. Qi, "A novel design and optimization method of an LCL filter for a shunt active power filter", *IEEE Transactions on Industrial Electronics* 61.8, (2014).

[20] M. Büyük, A. Tan, K. c. Bayindir, M. Tümay, "Analysis and Comparison of Passive Damping Methods for Shunt Active Power Filter with Output LCL Filter", *IEEE International Conference Acemp-Optim-Electromotion*, 2015.

[21] L. Asiminoaei, E. Aeloiza, P. N. Enjeti, F. Blaabjerg, "Shunt active-power-filter topology based on parallel interleaved inverters", *IEEE Trans. Ind. Electron.*, vol. 55, no. 3, pp. 1175-1189, Mar. 2008.

[22] P. Dey, S. Mekhilef, "Current controllers of active power filter for power quality improvement: a technical analysis", Automatika, vol. 56, no. 1, 2015.

[23] C. Lombard and A. P. J. Rens. "Evaluation of system losses due to harmonics in medium voltage distribution networks", *Energy Conference (ENERGYCON), 2016 IEEE International*, 2016.

[24] Patel, Pinkal J., Rajesh M. Patel, and Vinod Patel. "A Review of Three Level Voltage Source Inverter Based Shunt Active Power Filter.", *International Journal of Innovative Research in Advanced Engineering*, 2014.

[25] Asiminoael, Lucian, Frede Blaabjerg, and Steffan Hansen. "Detection is key-Harmonic detection methods for active power filter applications." *IEEE Industry Applications Magazine*, 2007.

[26] A. Ovalle, G. Ramos, S. Bacha, A. Hably, A. Rumeau, "Decentralized control of voltage source converters in microgrids based on the application of instantaneous power theory", *IEEE Trans. Ind. Electron.*, vol. 62, no. 2, pp. 1152-1162, Feb. 2015.

[27] P.Karuppanan and K. Mahapatra. "PLL with PI, PID and fuzzy logic controllers based shunt active power line conditioners." *Power Electronics, Drives and Energy Systems (PEDES) & 2010 Power India, 2010 Joint International Conference on*. IEEE, 2010.

[28] I. Colak, "Review of multilevel voltage source inverter topologies and control schemes", *Energy Convers. Manage.*, vol. 52, pp. 1114-1128, 2011.

[29] J. Huang and K.Corzine, "Extended operation of flying capacitor multilevel inverters", *IEEE Transactions on Power Electronics* 21.1., 2006.

[30] R. MUSA, "Improving the safety operation of three-phase shunt active filter", PhD Thesis, École de technologie supérieure, 2017.

[31] A. Al-Zamil and D. Torrey, "A passive series, active shunt filter for high power applications", *IEEE Transactions on Power Electronics* 16.1, 2001.

[32] N. Mohan, T.M. Undeland and W.P. Robbins, *"Power Electronics: Converters, Applicants and Design"* John Wiley & Sons, 1989.
[33] M. Rastogi, R. Naik, and N. Mohan. "A comparative evaluation of harmonic reduction techniques in three-phase utility interface of power electronic loads" *Industry Applications Society Annual Meeting Conference*, IEEE, 1993.

[34] A. H. Budhrani, K. J. Bhayani, and A. R. Pathak. "Design Parameters of Shunt Active Filter for Harmonics Current Mitigation." (2018).

[35] Wang, Yu, et al. "A Simplified Minimum DC-Link Voltage Control Strategy for Shunt Active Power Filters." *Energies* 11.9 (2018): 2407.

[36] R. Sriranjani, and S. Jayalalitha. "Design Of Shunt Active Filter Using Iterative Method To Mitigate The Harmonics And Reactive Power.", *arpnjournals*, 2006.

[37] S. Ponnaluri and A. Brickwedde. "Generalized system design of active filters." *Power Electronics Specialists Conference, 2001. PESC. 2001 IEEE 32nd Annual*. Vol. 3. IEEE, 2001.

[38] I. Etxeberria, "Sur les systèmes de l'électronique de puissance dédiés à la distribution électrique– Application à la qualité de l'énergie". *Diss. Institut National Polytechnique de Grenoble-INPG*, 2003.

[39] K. Chatterjee, B. G. Fernandes, and G. Dubey. "An instantaneous reactive volt-ampere compensator and harmonic suppressor system." *IEEE Transactions on Power Electronics*14.2 (1999): 381-392.

[40] C.Y. Hsu and H.Y. Wu. "A new single-phase active power filter with reduced energy-storage capacity." *IEE Proceedings-Electric Power Applications* 143.1, 1996.

[41] Abb.com, " Active Filters - PQFI-PQFM-PQFS ", 2018. [Online]. Available: https://search-ext.abb.com/library/Download.aspx?DocumentID=9AKK107046A1970&LanguageCode=en&DocumentPartId=&Action=Launch. [Accessed: Nov. 8, 2018].

[42] A.F. Zobaa, "Comparing power factor and displacement factor corrections based on IEEE Std. 18-2002." *Harmonics and Quality of Power, 2004. 11th International Conference on*. IEEE, 2004.

[43] M. Mamo, and A. Merid, "Power Quality assessment and mitigation at Walya-Steel Industries and Ethio-Plastic share company." *Zede Journal* 31, 2014.

[44] Dugan, *Electrical power systems quality*. Vol. 2. New York: mcgraw-Hill, 1996.

[45] R. Pregitzer, J.G Pinto, L. Monteiro and J. Afonso, "Shunt active power filter with dynamic output current limitation." *Industrial Electronics, 2007. ISIE 2007. IEEE International Symposium*, IEEE, 2007.

[46] Guillod, Thomas, Florian Krismer, and Johann W. Kolar. "Protection of MV converters in the grid: the case of MV/LV solid-state transformers." *IEEE Journal of Emerging and Selected Topics in Power Electronics* 5.1, 2017.

[47] Glover, J. Duncan, M. Sarma, and T. Overbye. *Power System Analysis & Design, SI Version*. Cengage Learning, 2012.

[48] IEEE Guide for Protecting Power Transformers, IEEE Standard C37.91- 2008, 2008.

[49] R. Hunt, J. Schaefer, and B. Bentert, "Practical experience in setting transformer differential inrush restraint." *61st Annual Conference for Protective Relay Engineers*. 2008.

[50] S. Biswas, R. Dash, K.Choudhury and S. Sahoo, "A review paper on inrush fault isolation methods of a three-phase transformer." *Technologies for Smart-City Energy Security and Power (ICSESP), 2018*. IEEE, 2018.

[51] B. Jiří and P. Martin, "Transformer inrush-Harmonics in the current." *2018 19th International Scientific Conference on Electric Power Engineering (EPE)*. IEEE, 2018.

[52] Schneider.com, "Role of Harmonic 2 setting in Earth fault protection setting", 2018. [Online]. Available: https://www.schneider-electric.com/resources/sites/SCHNEIDER_ELECTRIC/content/live/-FAQS /272000/FA272173/en_US/FA272173.pdf . [Accessed: Nov. 24, 2018].

[53] Abb.com, "Switching to higher performance", 2018. [Online]. Available: https://library.e.abb.com /public/685ed95a8abe9a61c12574b9002fd099/19-24%203m801_ENG72dpi.pdf. [Accessed:Jan.11, 2018].